Nanoscale III-V CMOS

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SEMI Advanced Semiconductor Manufacturing Conference

Saratoga Springs, NY; May 16-19, 2016

Acknowledgements:

- Students and collaborators: D. Antoniadis, J. Lin, W. Lu, A. Vardi, X. Zhao
- Sponsors: Applied Materials, DTRA, KIST, Lam Research, Northrop Grumman, NSF, Samsung
- Labs at MIT: MTL, EBL

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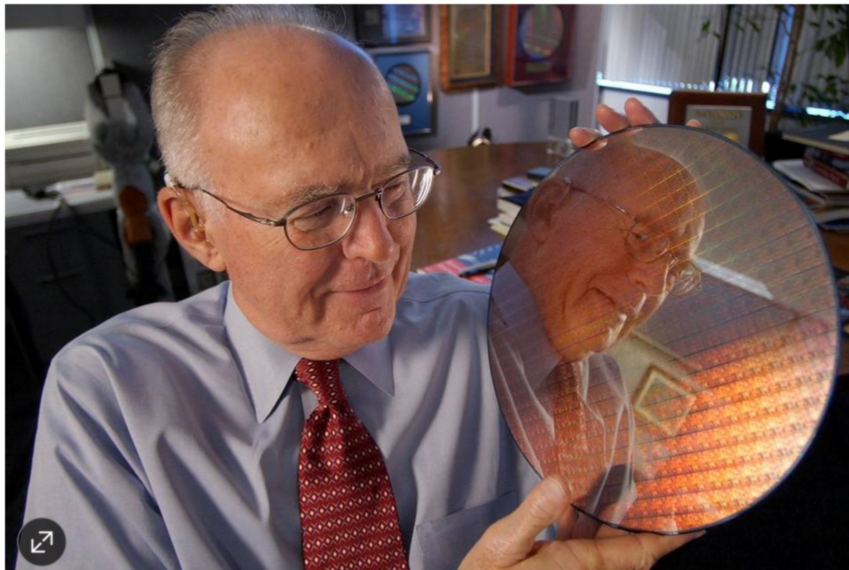
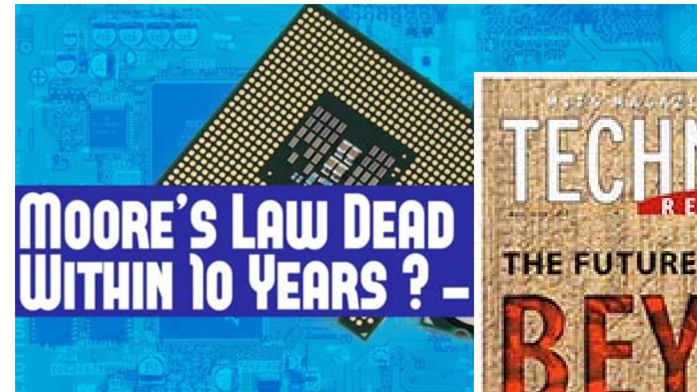
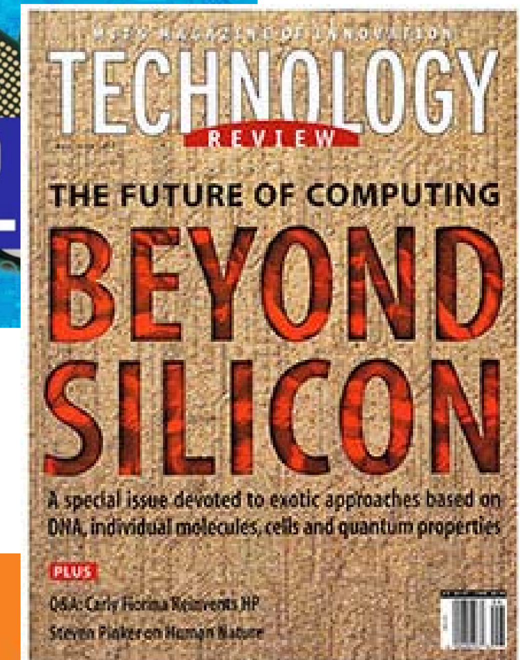
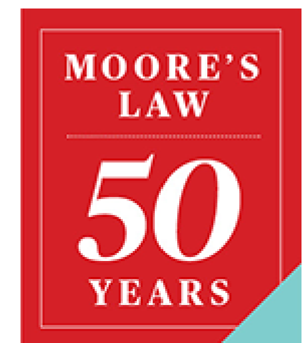
1. Moore's Law at 50: the end in sight?



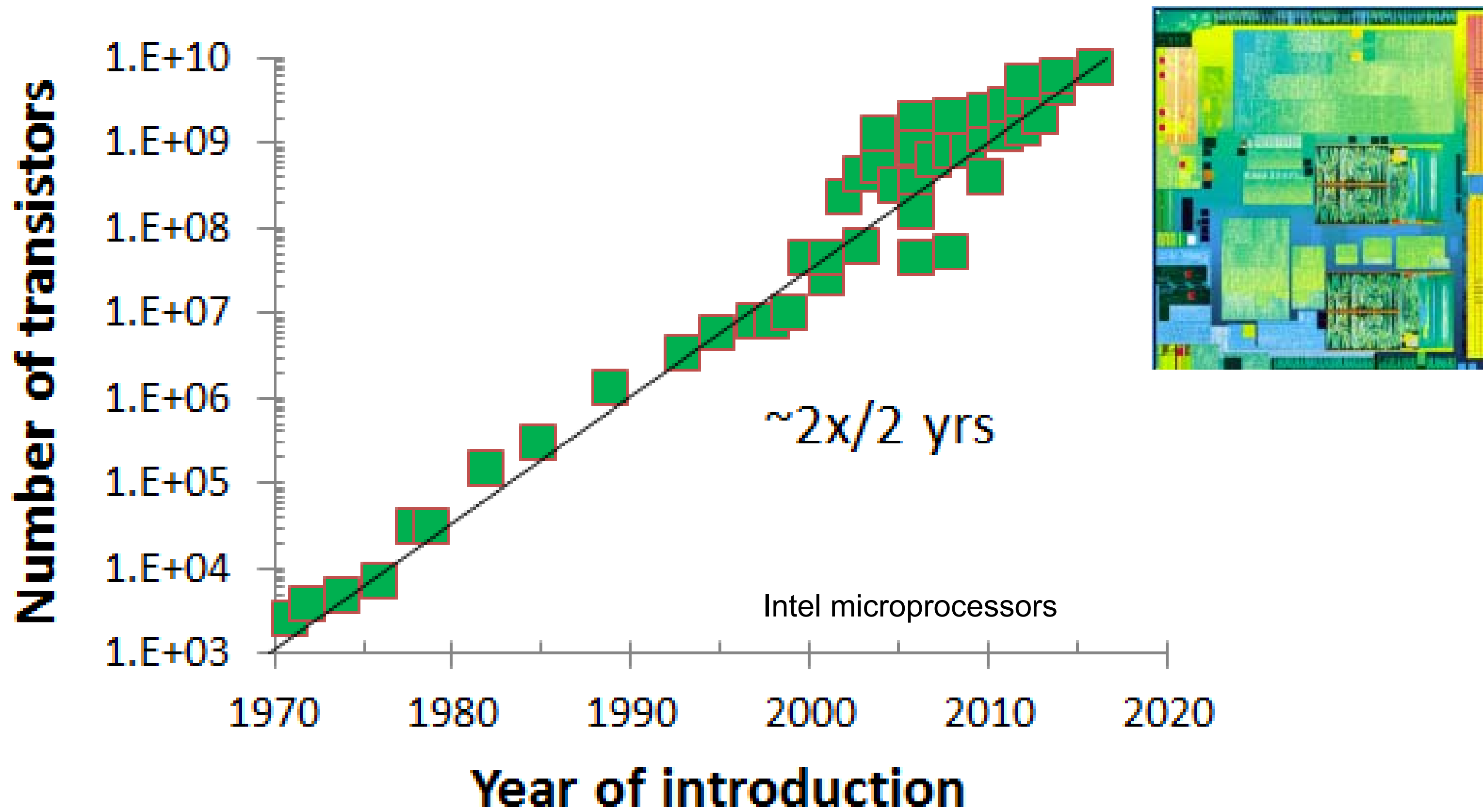






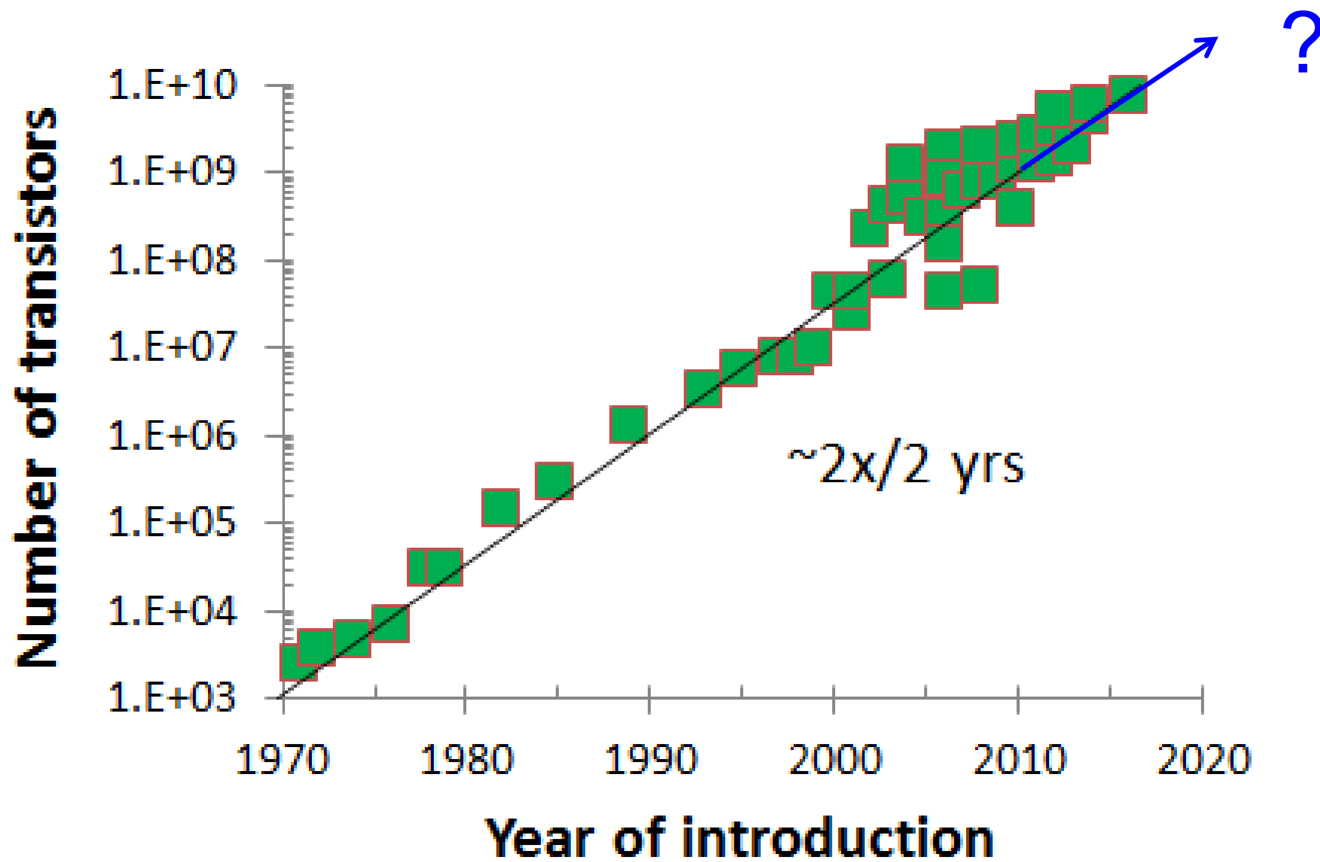
Moore’s Law

Moore’s Law = exponential increase in transistor density



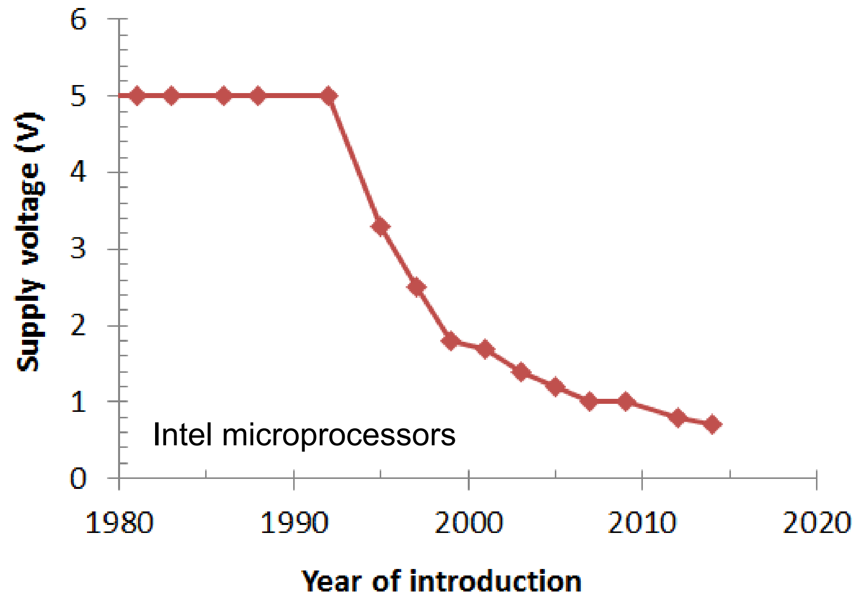
Moore's Law

How far can Si support Moore's Law?

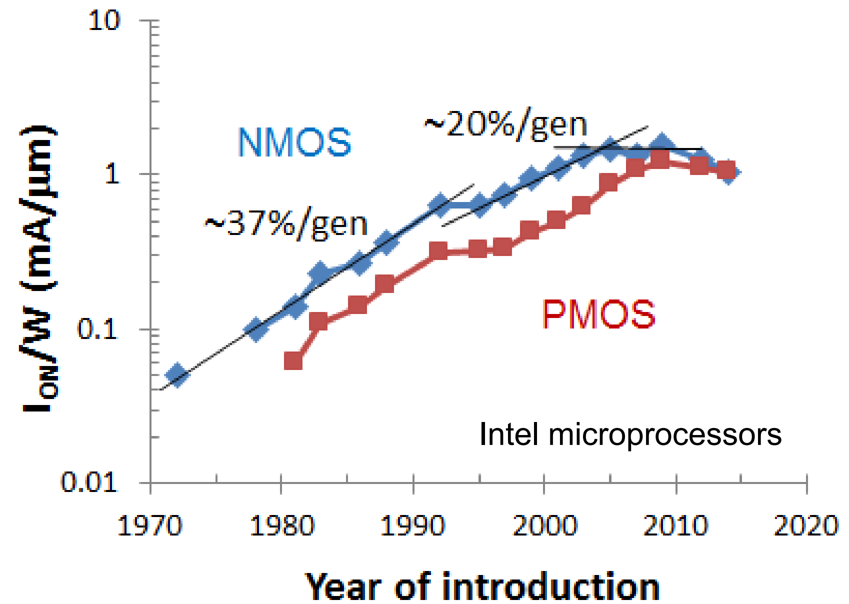


Transistor scaling → Voltage scaling → Performance suffers

Supply voltage:



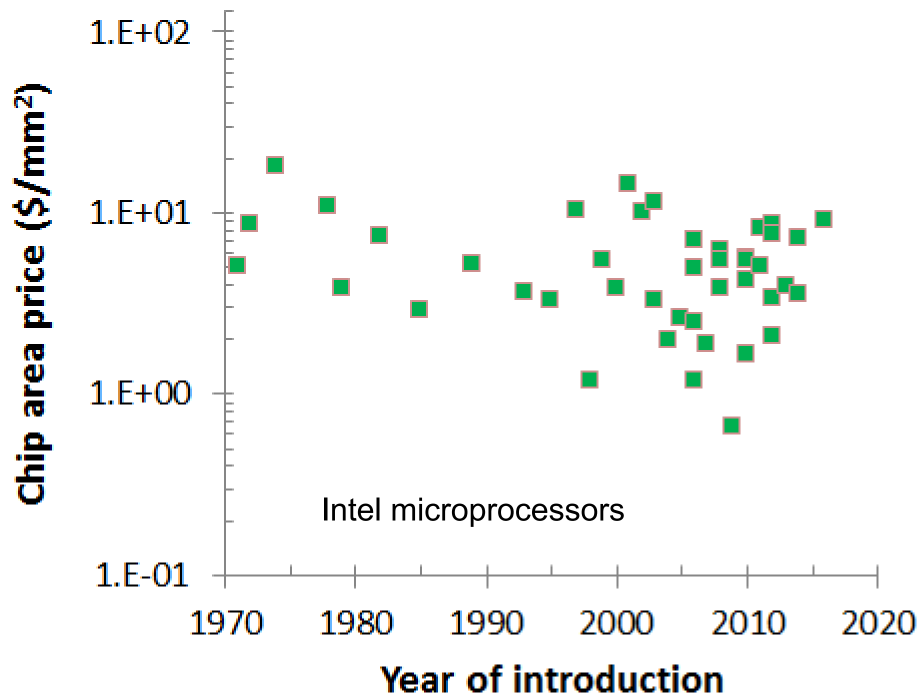
Transistor current density:



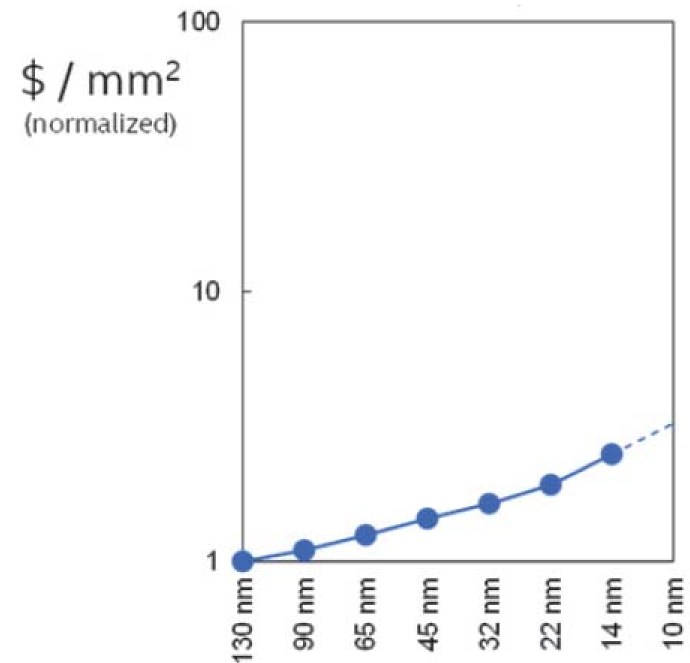
Transistor performance saturated in recent years

Chip Price vs. Chip Cost

Chip area price:



Chip area cost:



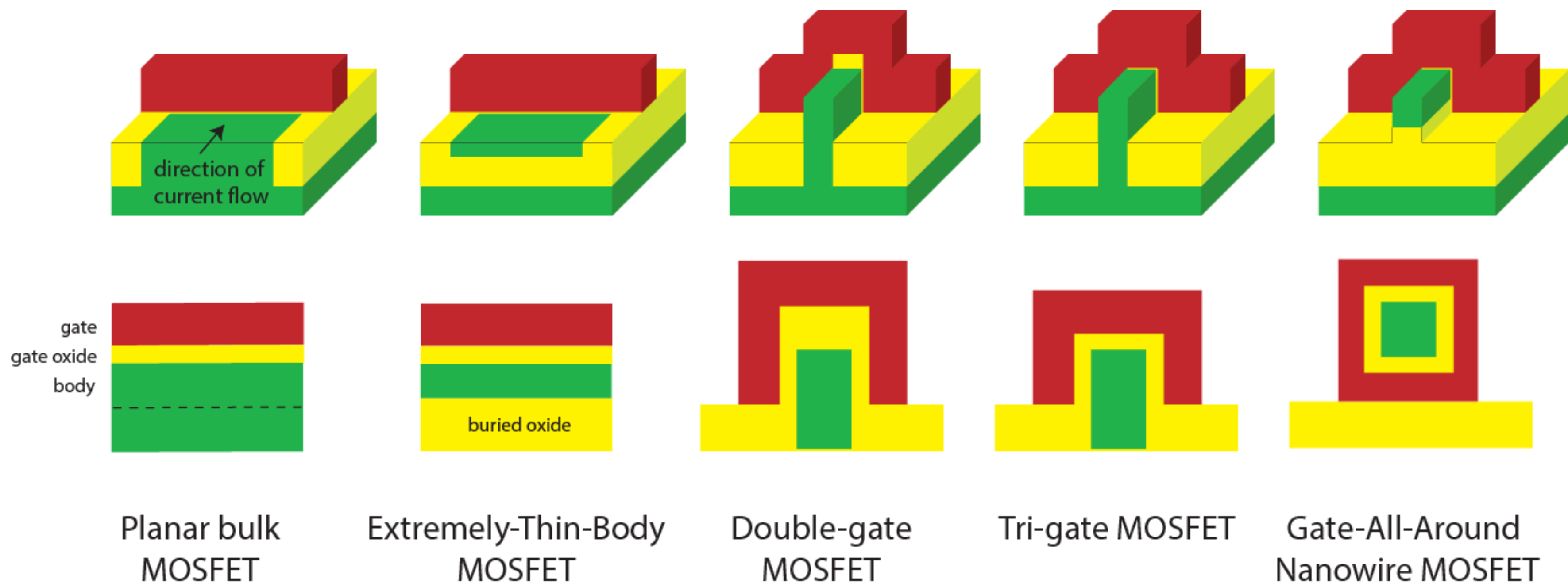
Holt, ISSCC 2016

Increasing chip cost might bring the end to Moore's Law

THE END IS NEAR.
YOU WISH.

Moore's Law:
it's all about MOSFET scaling

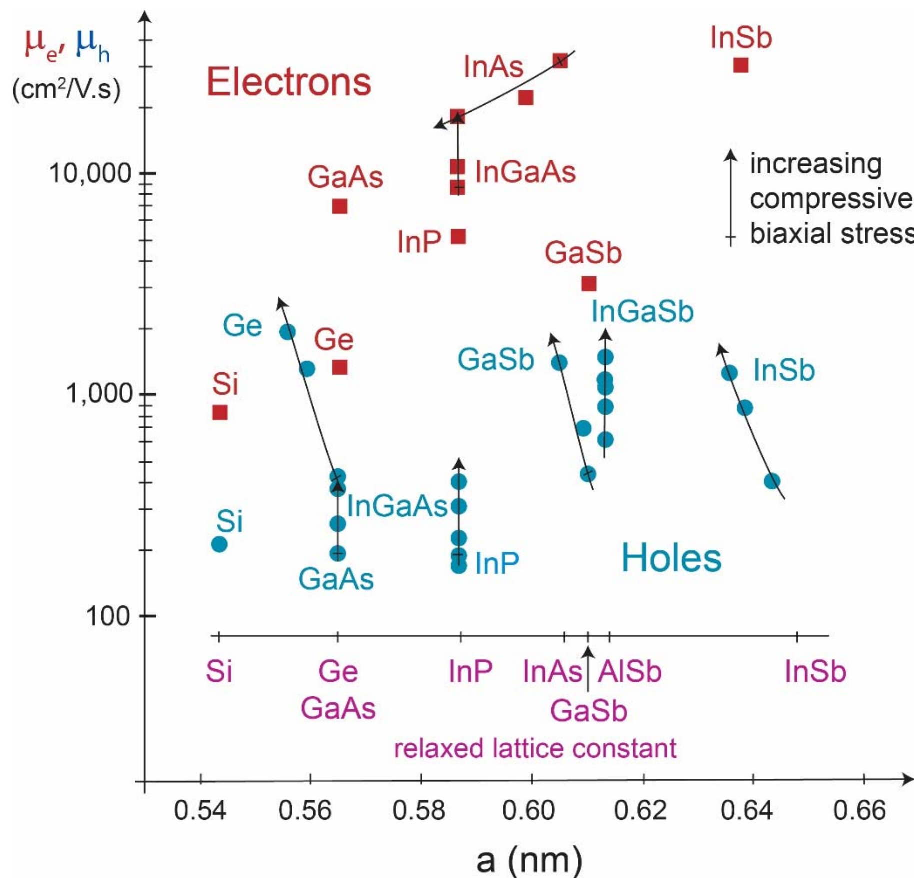
1. New device structures:



Enhanced gate control → improved scalability

Moore's Law: it's all about MOSFET scaling

2. New materials:



n-channel:

Si → Strained Si → SiGe → InGaAs

p-channel:

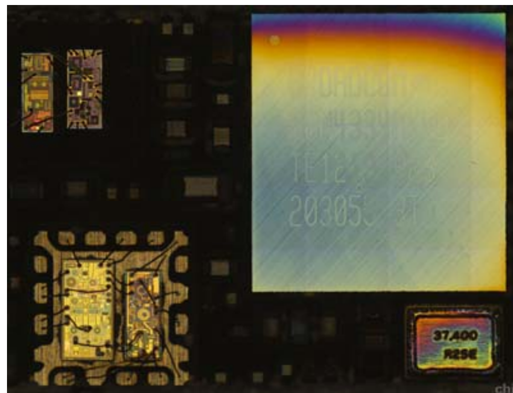
Si → Strained Si → SiGe → Ge → InGaSb

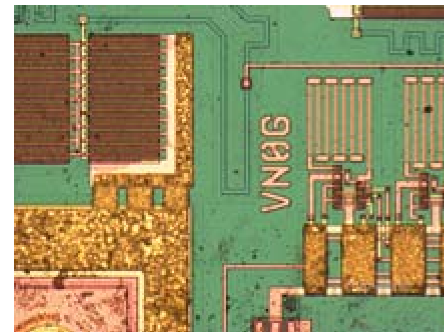
Future CMOS might involve:

- two different channel materials
- with **two different relaxed lattice constants**!

del Alamo, Nature 2011 (updated)

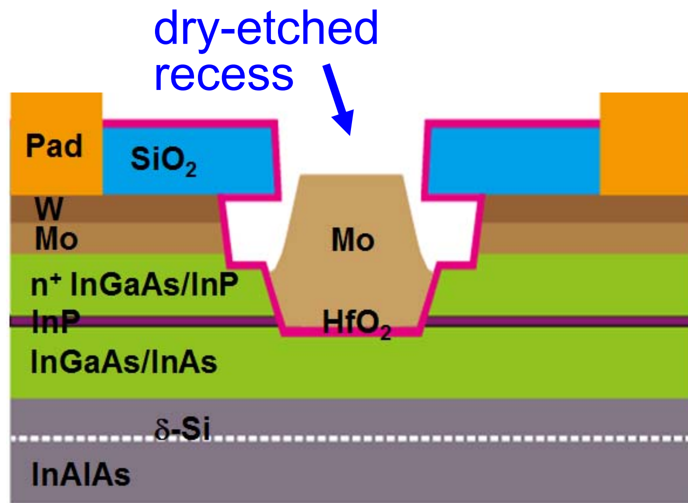
III-V electronics in your pocket!



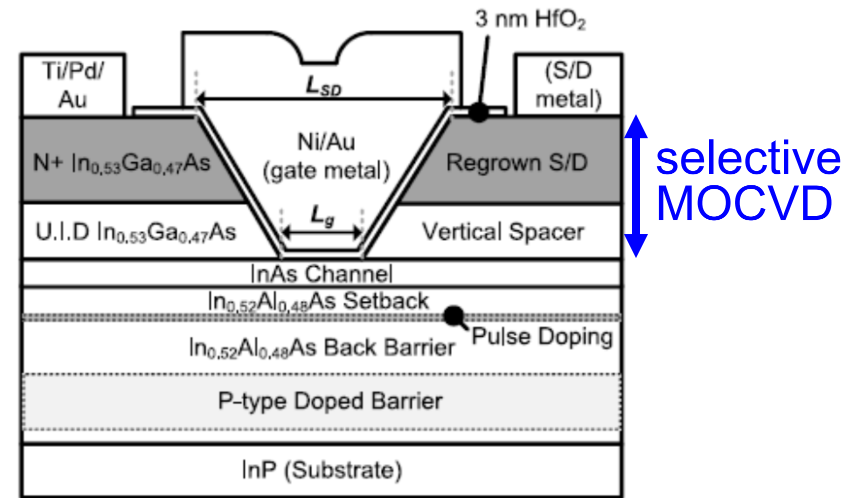


2. Self-aligned Planar InGaAs MOSFETs

dry-etched recess



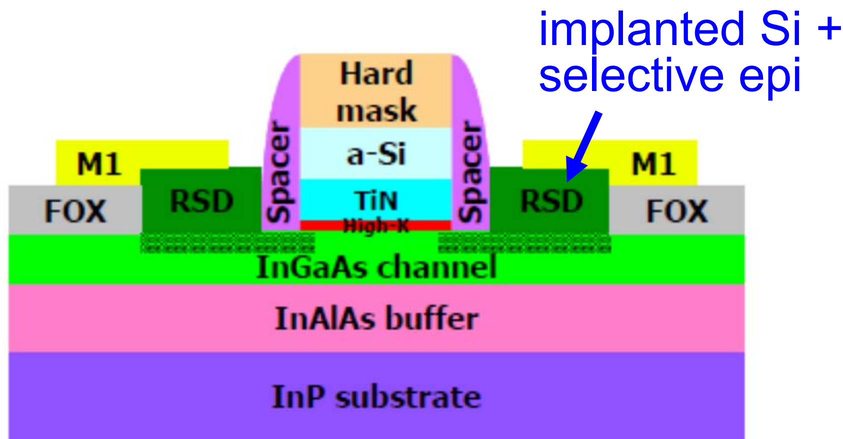
Lin, IEDM 2012, 2013, 2014



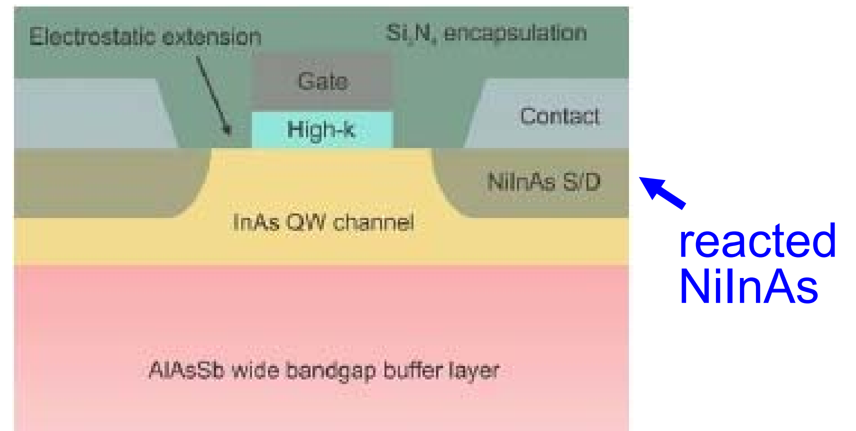
selective MOCVD

Lee, EDL 2014; Huang, IEDM 2014

implanted Si + selective epi



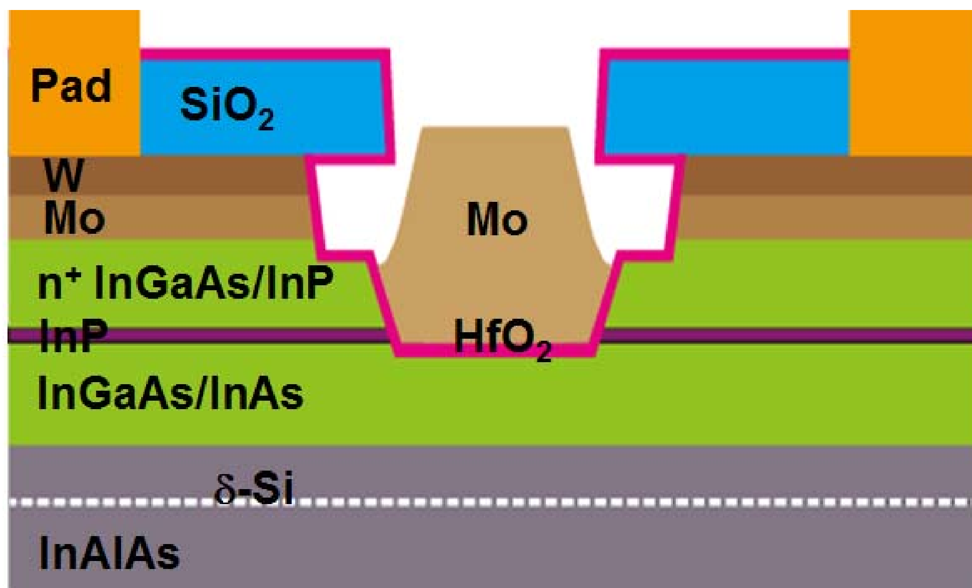
Sun, IEDM 2013, 2014

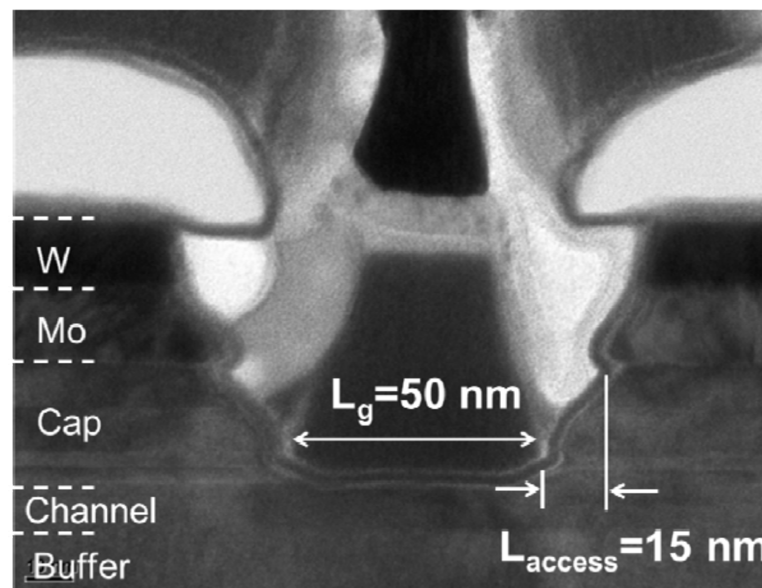


reacted NiInAs

Chang, IEDM 2013

Self-aligned Planar InGaAs MOSFETs @ MIT





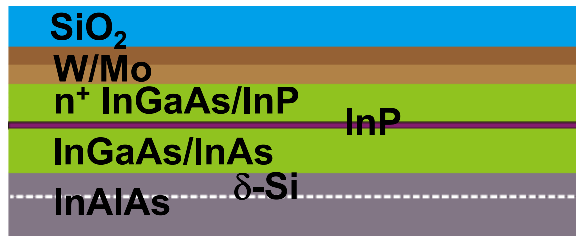
Lin, IEDM 2012, 2013, 2014

Recess-gate process:

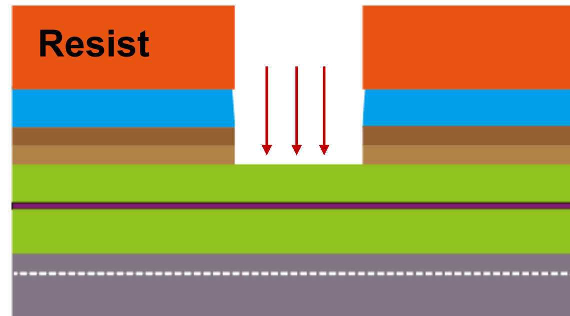
- CMOS-compatible
- Refractory ohmic contacts (W/Mo)
- Extensive use of RIE

Fabrication process

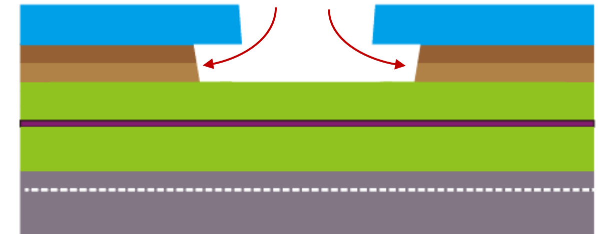
Mo/W ohmic contact
+ SiO_2 hardmask



SF_6, CF_4 anisotropic RIE

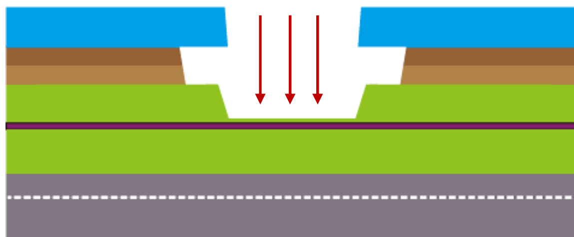


CF_4:O_2 isotropic RIE

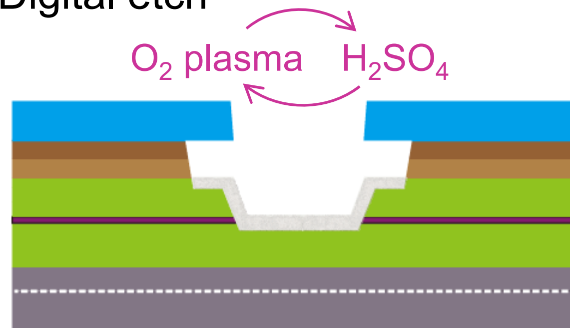


Waldron, IEDM 2007

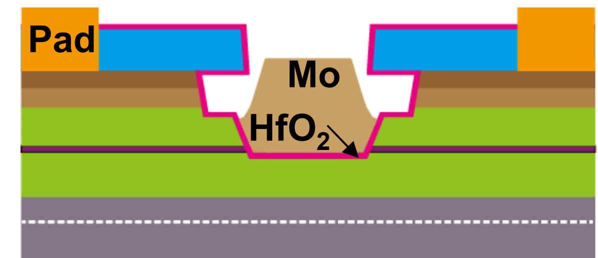
Cl_2:N_2 anisotropic RIE



Digital etch



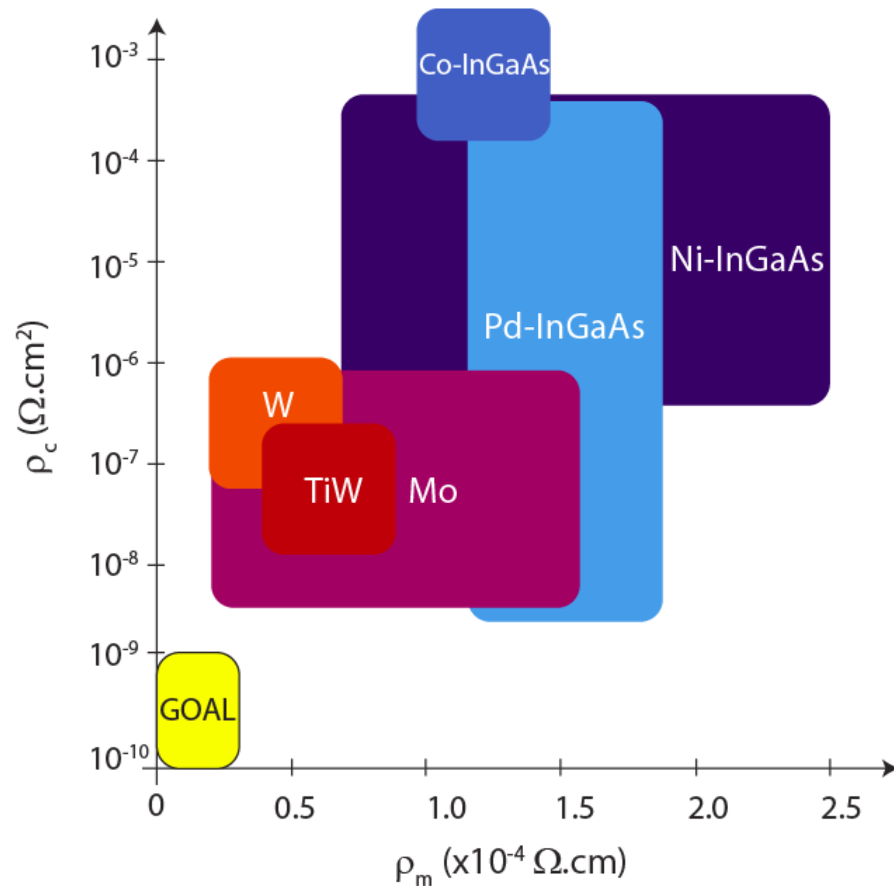
Finished device



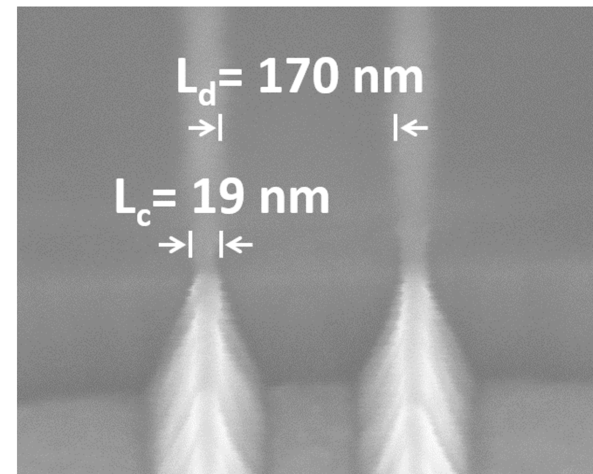
Lin, EDL 2014

- Ohmic contact first, gate last
- Precise control of vertical (~1 nm), lateral (~5 nm) dimensions
- MOS interface exposed late in process

Mo Nanoscale Contacts



Mo on n^+-$In_{0.53}Ga_{0.47}As$:

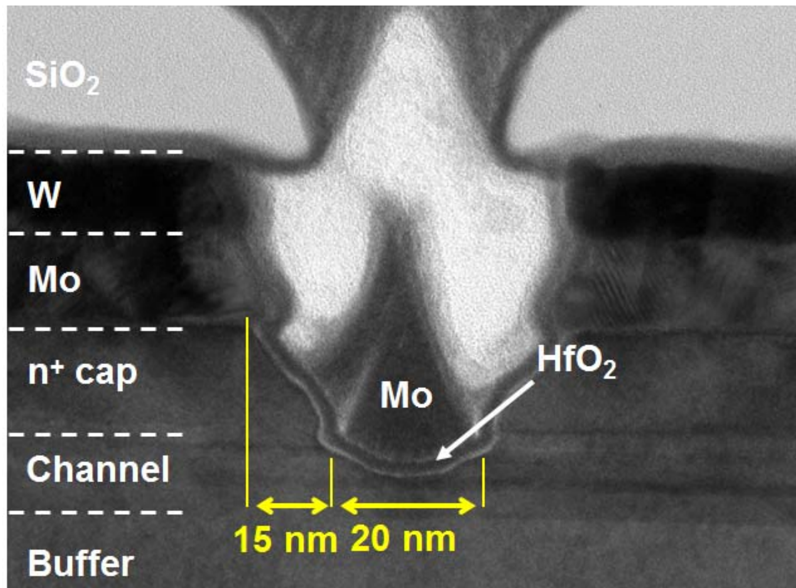


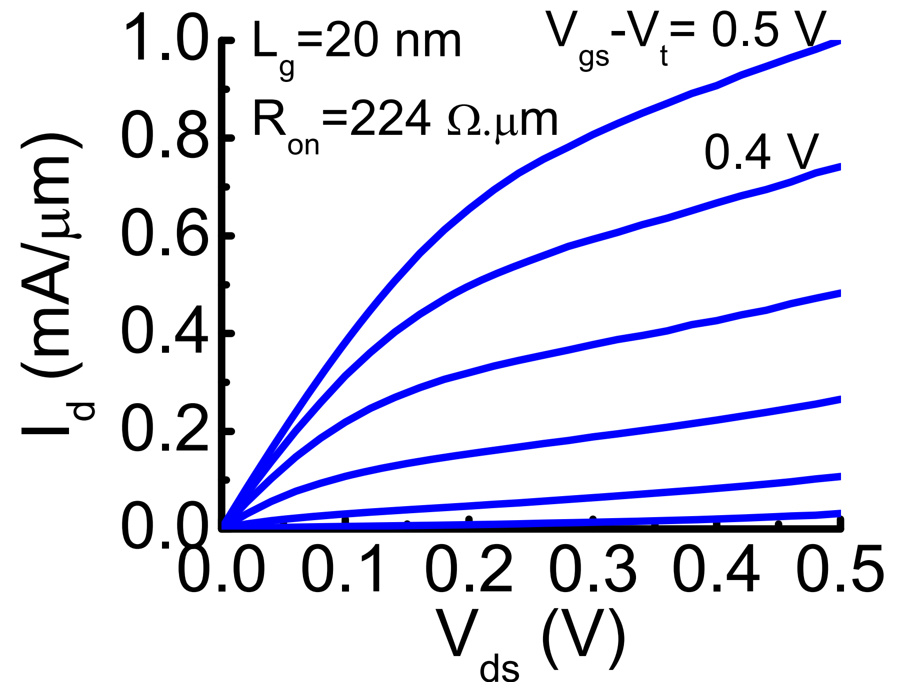
$R_c \sim 40\ \Omega.\mu m$ for $L_c \sim 20$ nm

- Need low ρ_c and ρ_m → Mo best contact system
- Average $\rho_c = 0.69\ \Omega.\mu m^2$

Lu, EDL 2014

L_g=20 nm InGaAs MOSFET





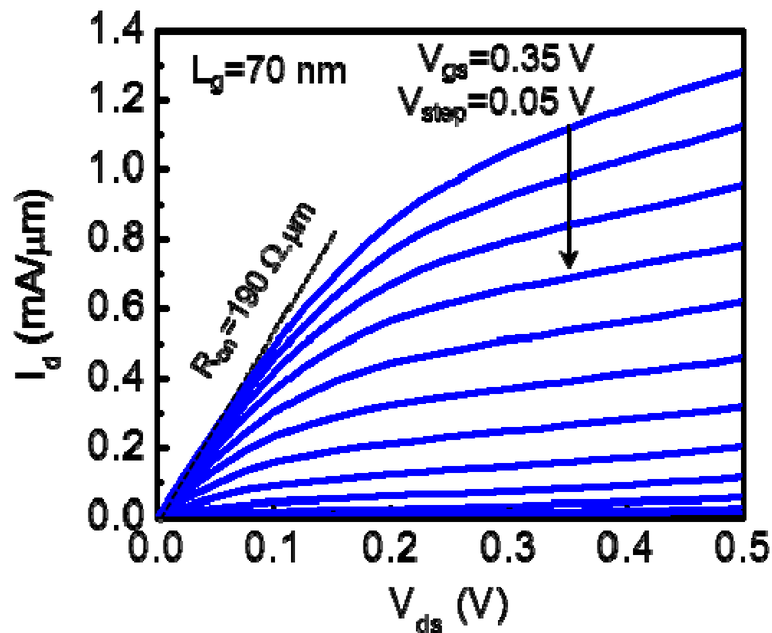
L_g = 20 nm, L_{access}= 15 nm MOSFET

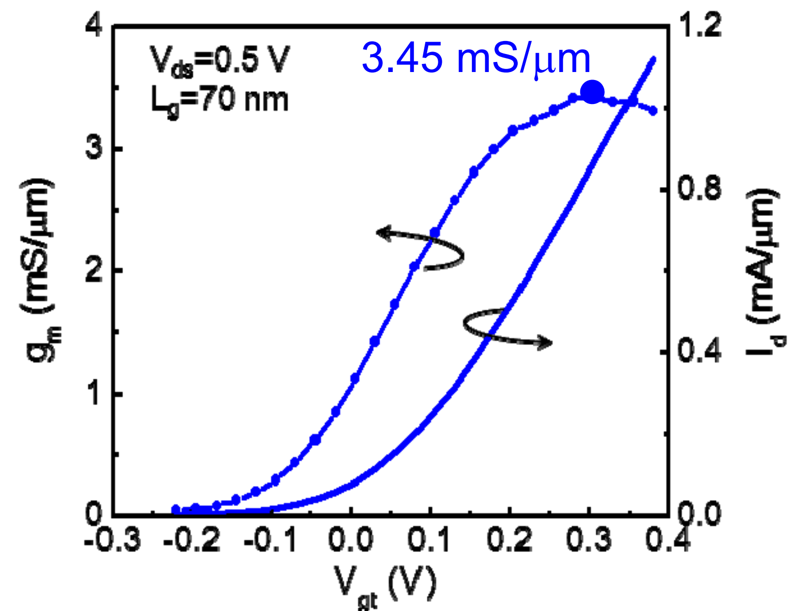
→ tightest III-V MOSFET made at the time

Lin, IEDM 2013

Highest performance InGaAs MOSFET

- Channel: $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$
- Gate oxide: HfO_2 (2.5 nm, EOT~ 0.5 nm)





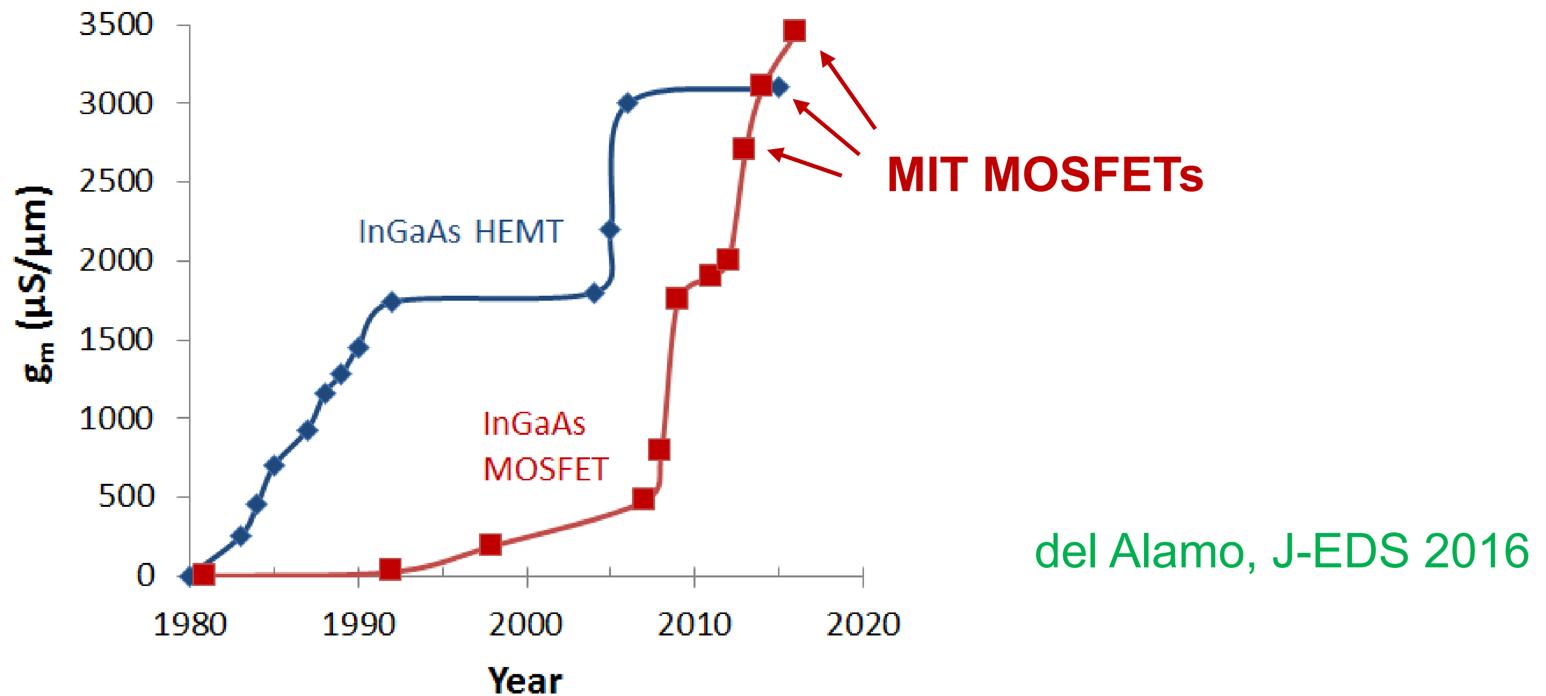
L_g=70 nm:

- Record $g_{m,max}$ = 3.45 mS/μm at V_{ds}= 0.5 V
- R_{on} = 190 Ω.μm

Lin, EDL 2016

Benchmarking: g_m in MOSFETs vs. HEMTs

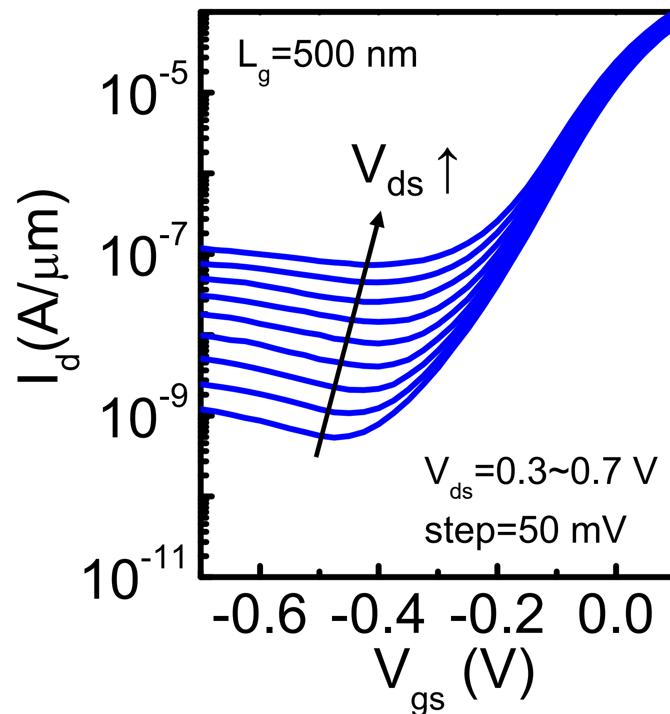
g_m of InGaAs MOSFETs vs. HEMTs (any V_{DD}, any L_g):

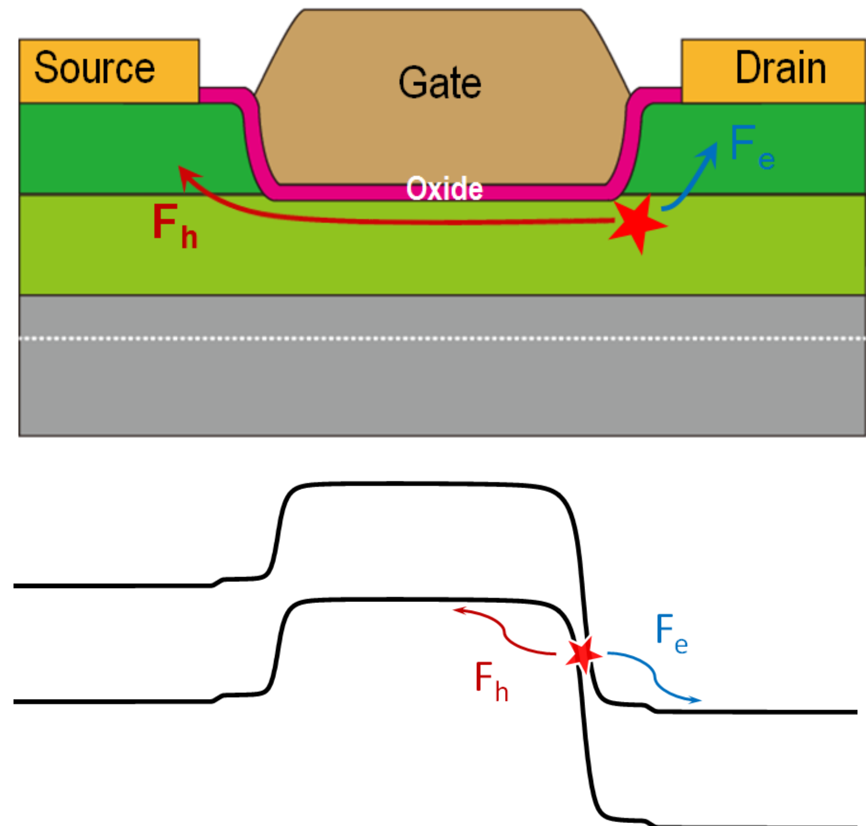


- InGaAs MOSFETs now superior to InGaAs HEMTs
- No sign of stalling → more progress ahead!

Excess OFF-state current

Transistor fails to turn off:



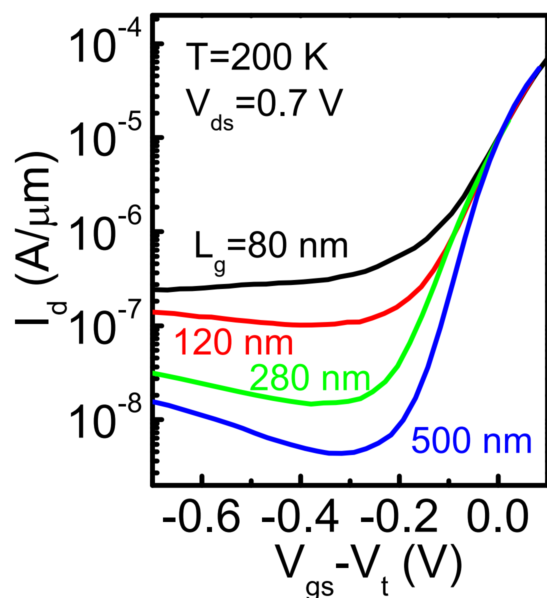


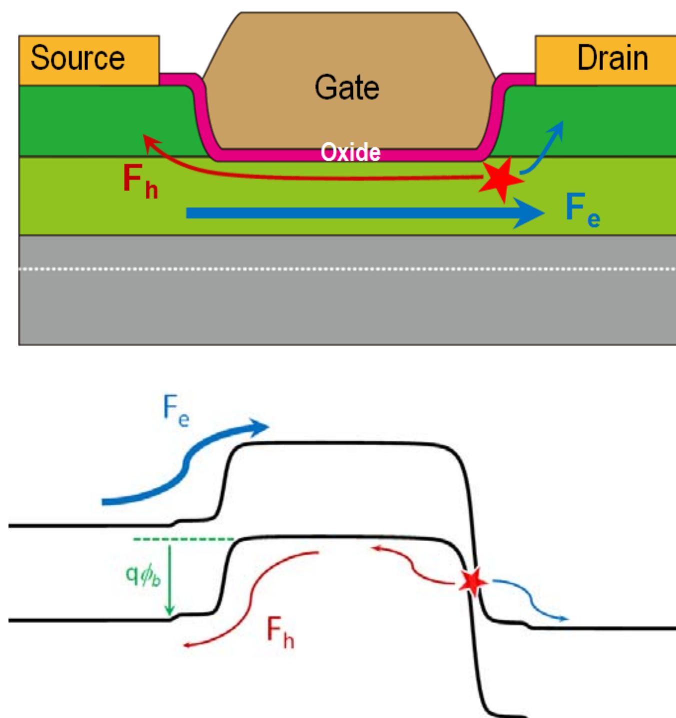
OFF-state current enhanced with V_{ds}

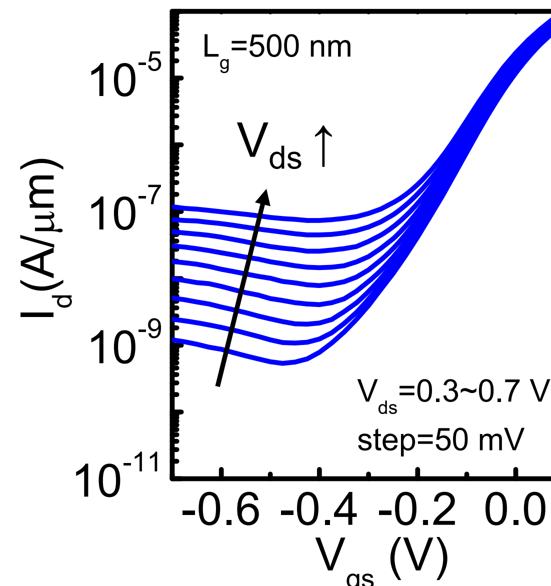
→ *Band-to-Band Tunneling (BTBT) or Gate-Induced Drain Leakage (GIDL)*

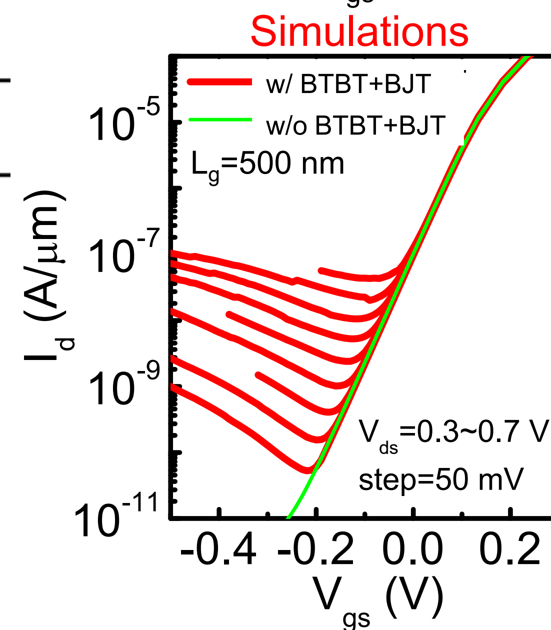
Lin, IEDM 2013

Excess OFF-state current









Lin, EDL 2014

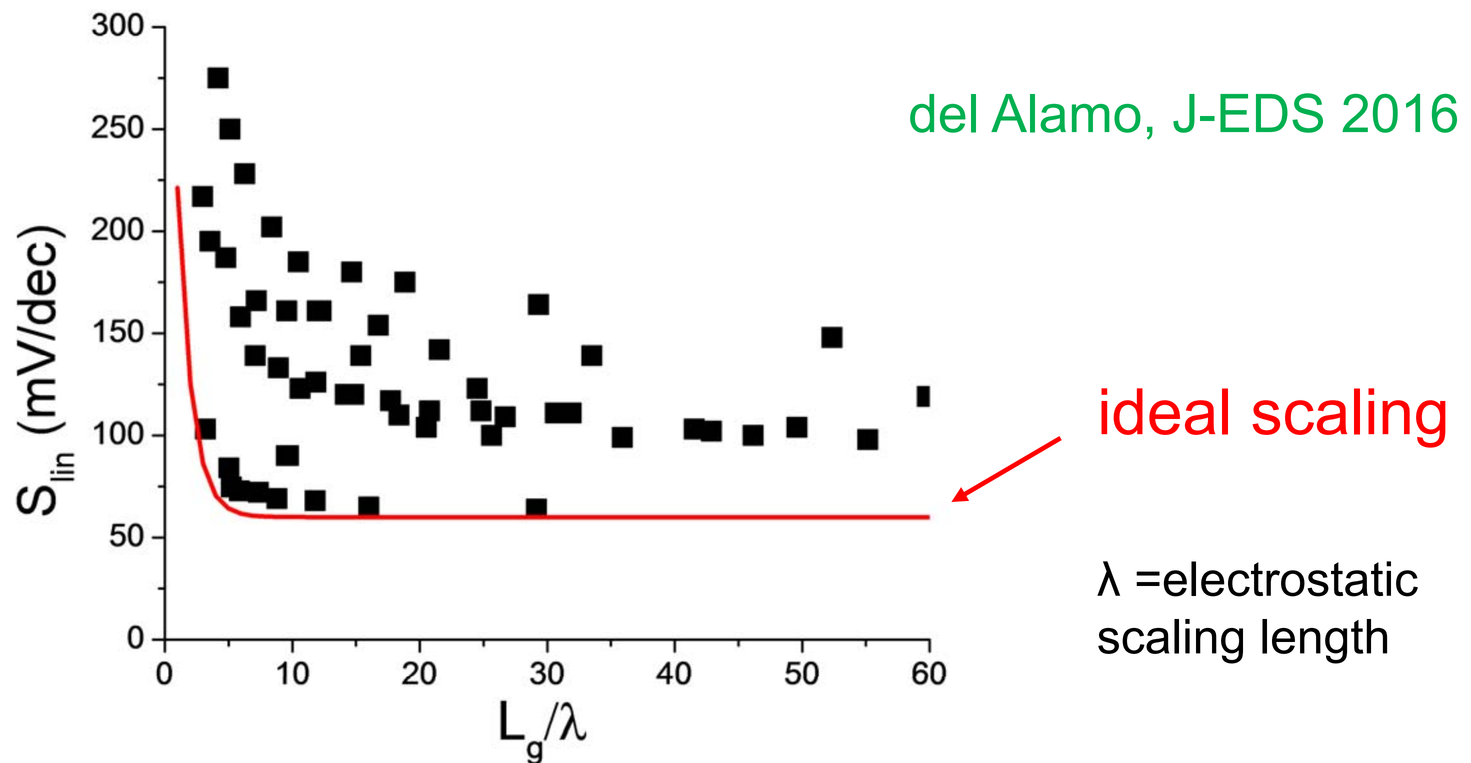
Lin, TED 2015

L_g↓ → OFF-state current ↑

→ additional *bipolar gain effect due to floating body*

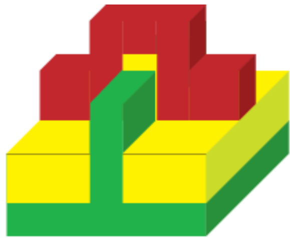
Planar MOSFET scaling limit

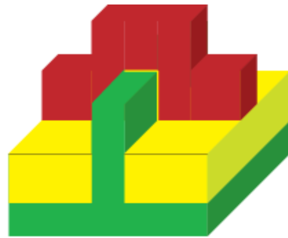
Scaling of linear subthreshold swing



- Nearly ideal electrostatic scaling behavior
- At limit of scaling around L_g~50 nm

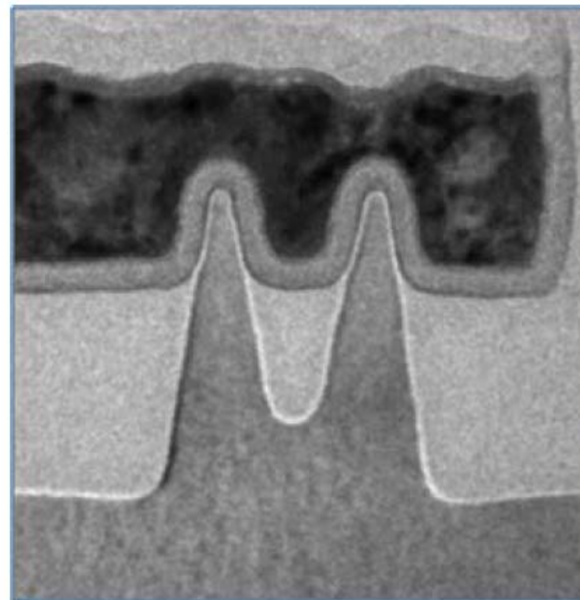
3. InGaAs FinFETs



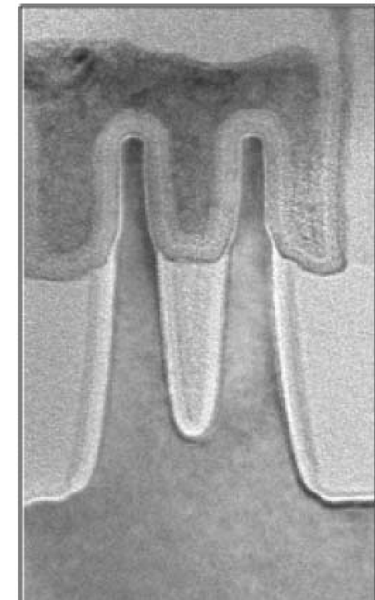


Double-gate MOSFET   Tri-gate MOSFET

Intel Si Trigate MOSFETs

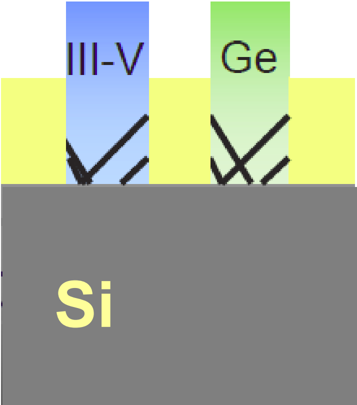


22 nm Process



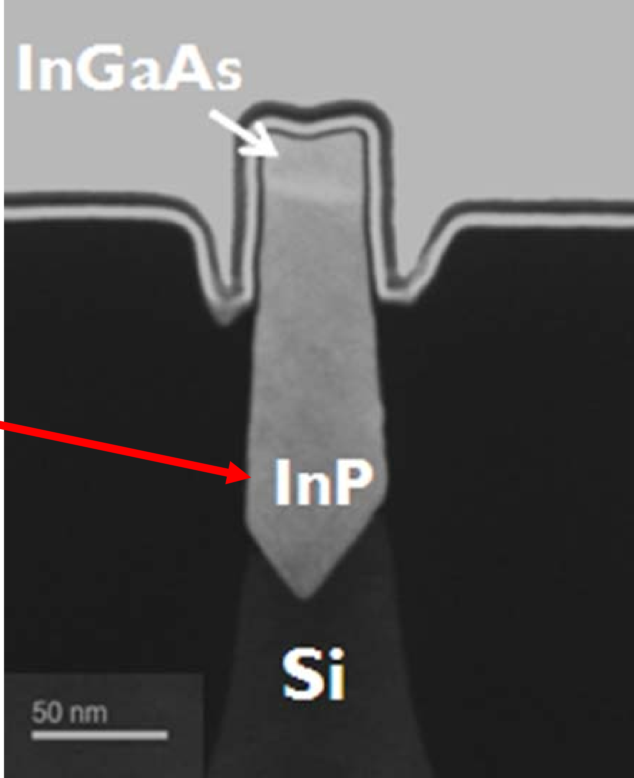
14 nm Process

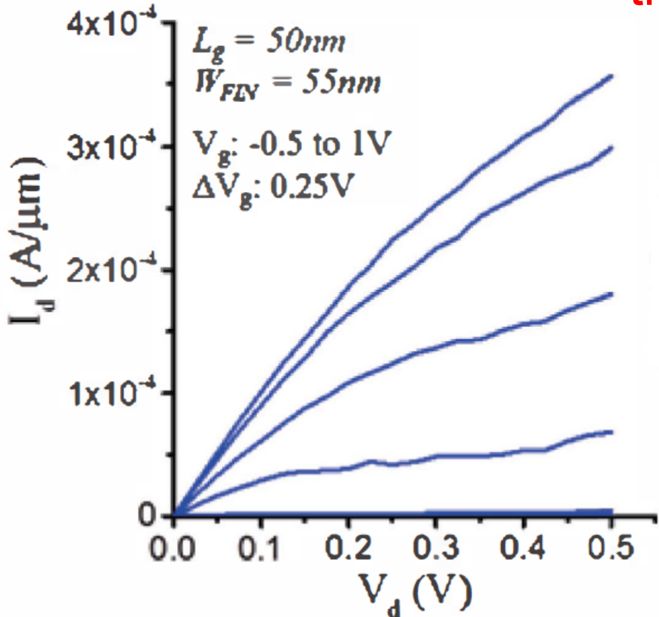
Bottom-up InGaAs FinFETs



Aspect-Ratio Trapping
Fiorenza, ECST 2010

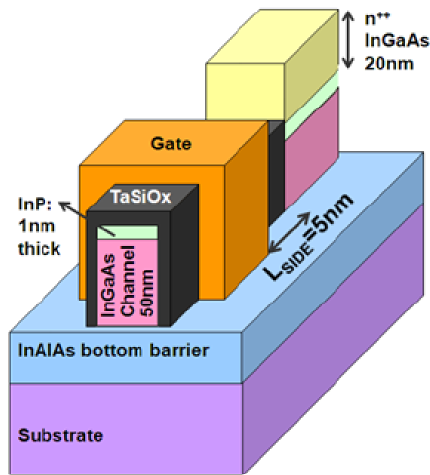
Epi-grown fin inside trench

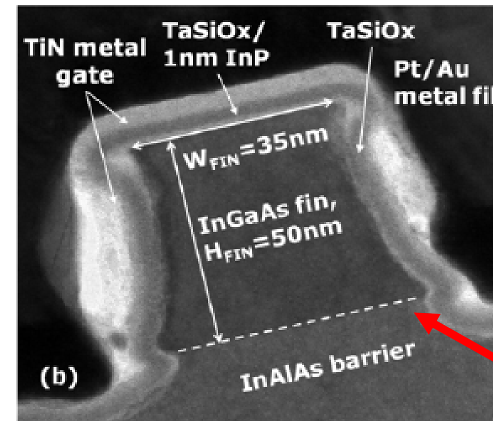




Waldron, VLSI Tech 2014

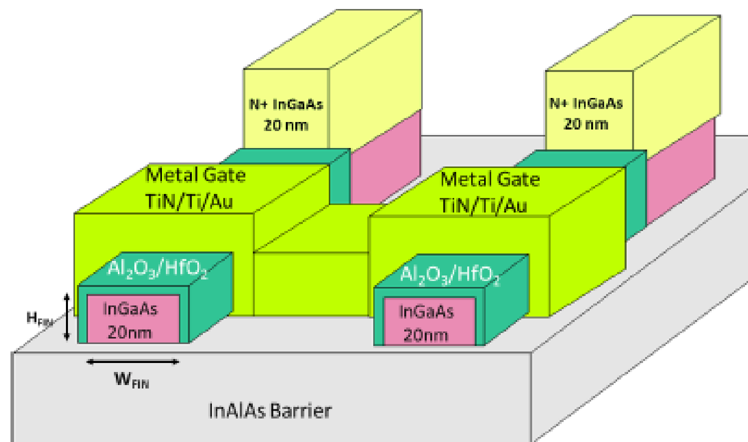
Top-down InGaAs FinFETs

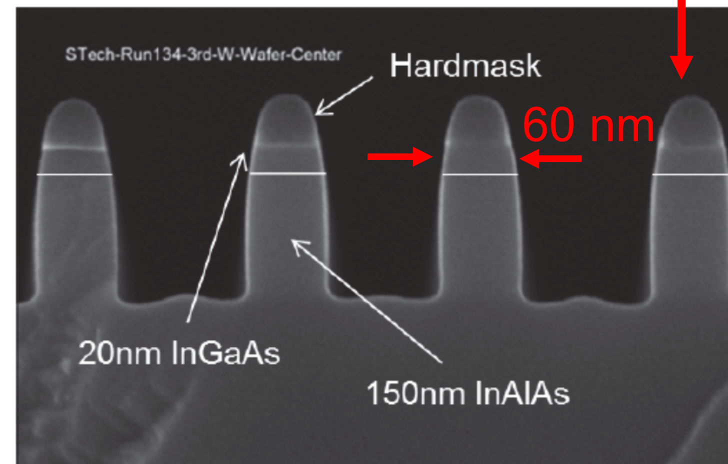




dry-etched fins

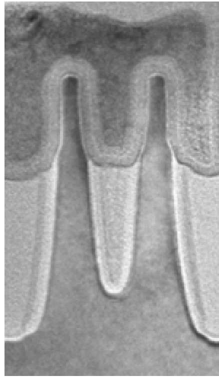
Radosavljevic, IEDM 2010



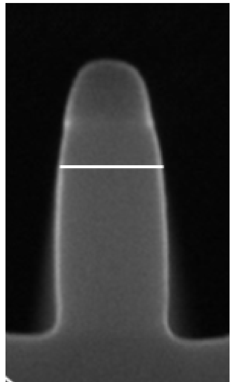


Kim, IEDM 2013

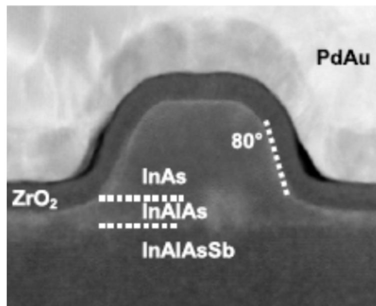
InGaAs FinFETs: g_m



Natarajan, IEDM 2014

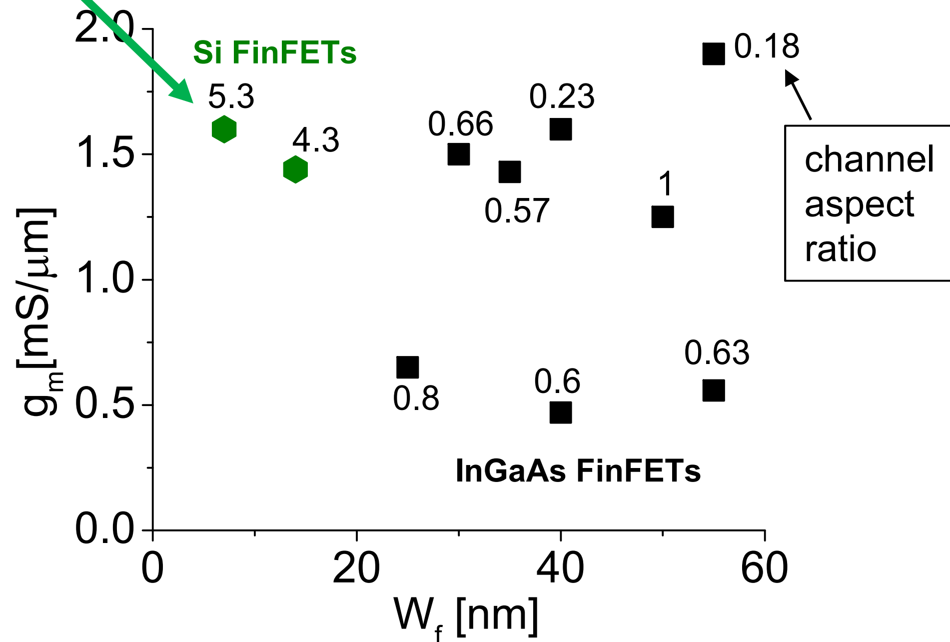


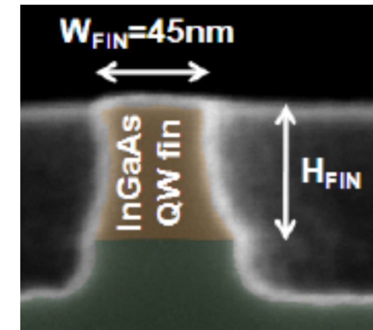
Kim, IEDM 2013



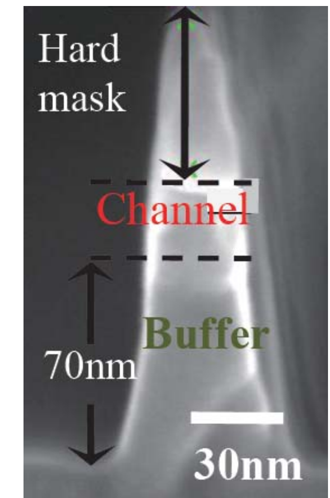
Oxland, EDL 2016

g_m per width of gate periphery





Radosavljevic, IEDM 2011

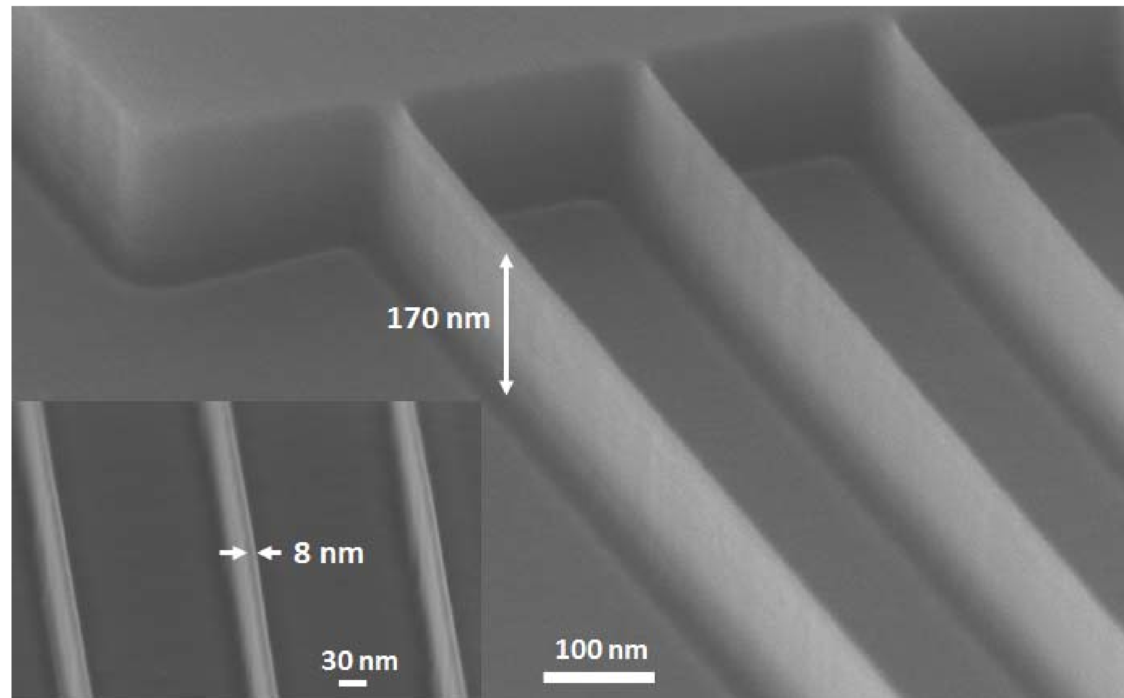


Thathachary, VLSI 2015

- Narrowest InGaAs FinFET fin: W_f=25 nm
- Best fin aspect ratio of InGaAs FinFET: 1
- g_m much lower than planar InGaAs MOSFETs

InGaAs FinFETs @ MIT

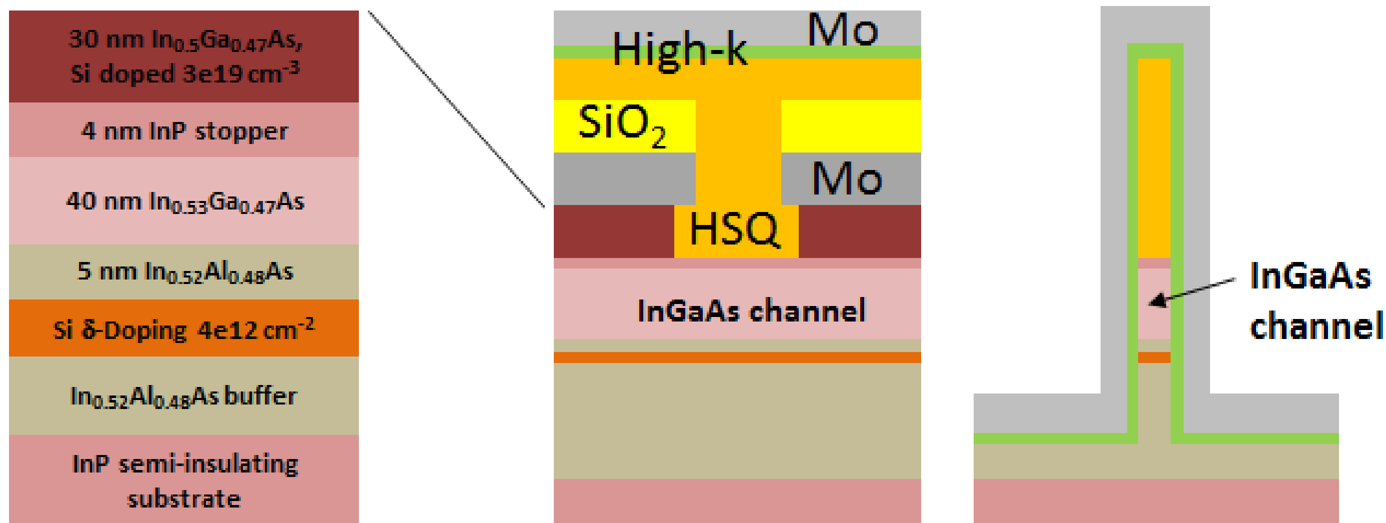
Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch



- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs Double-Gate MOSFET

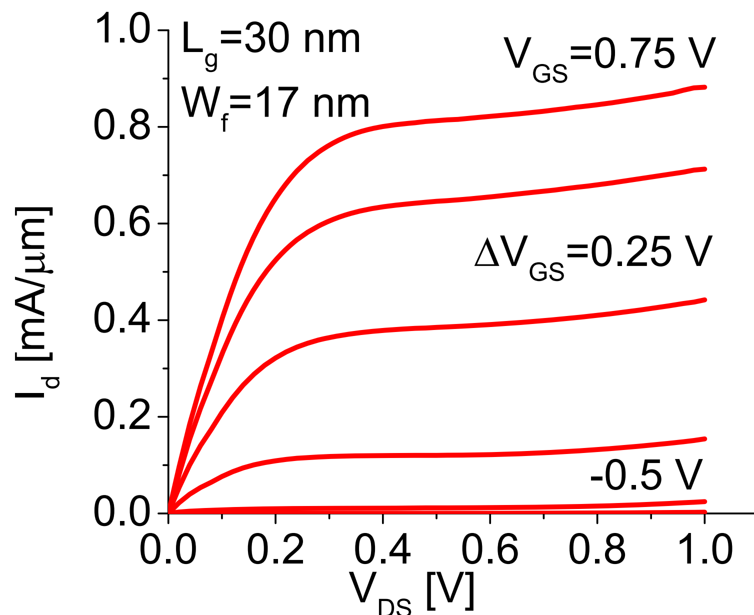


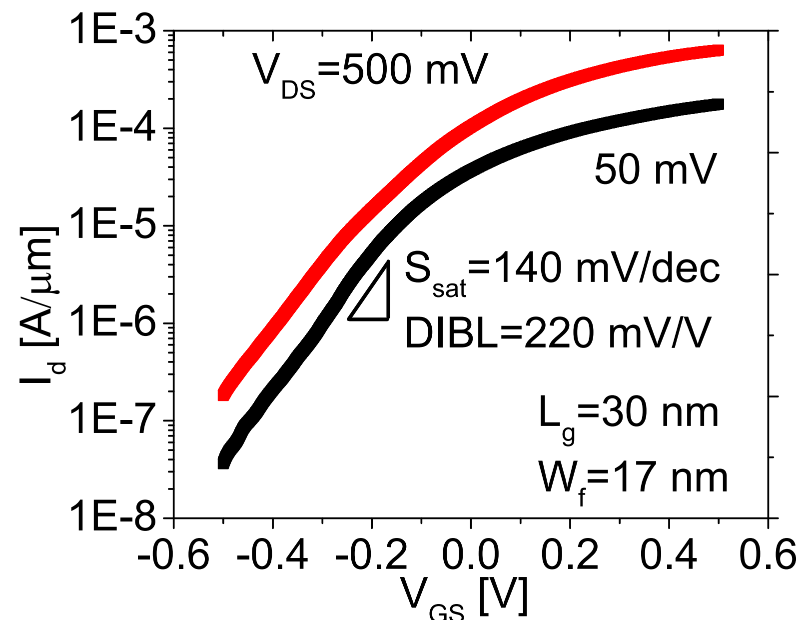
Vardi, VLSI 2016

- CMOS compatible process
- Mo contact-first process
- Fin mask left in place → double-gate MOSFET

InGaAs Double-Gate MOSFET

L_g=30 nm, W_f=17 nm, H_c=40 nm (AR=2.3):



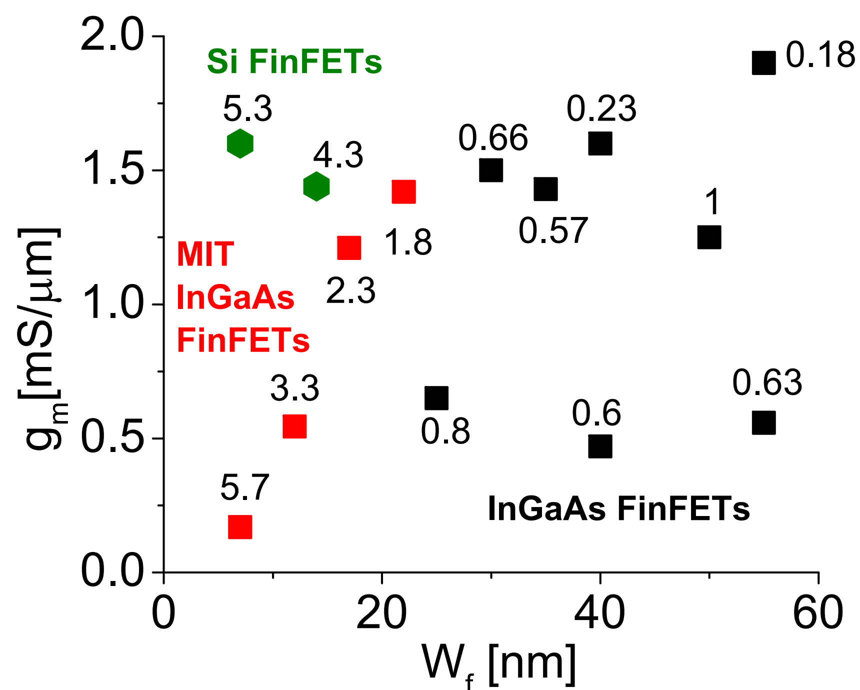


- g_m=1.12 mS/µm
- R_{on}=230 Ω.µm
- S_{sat}=140 mV/dec

Vardi, VLSI 2016

InGaAs FinFETs: g_m benchmarking

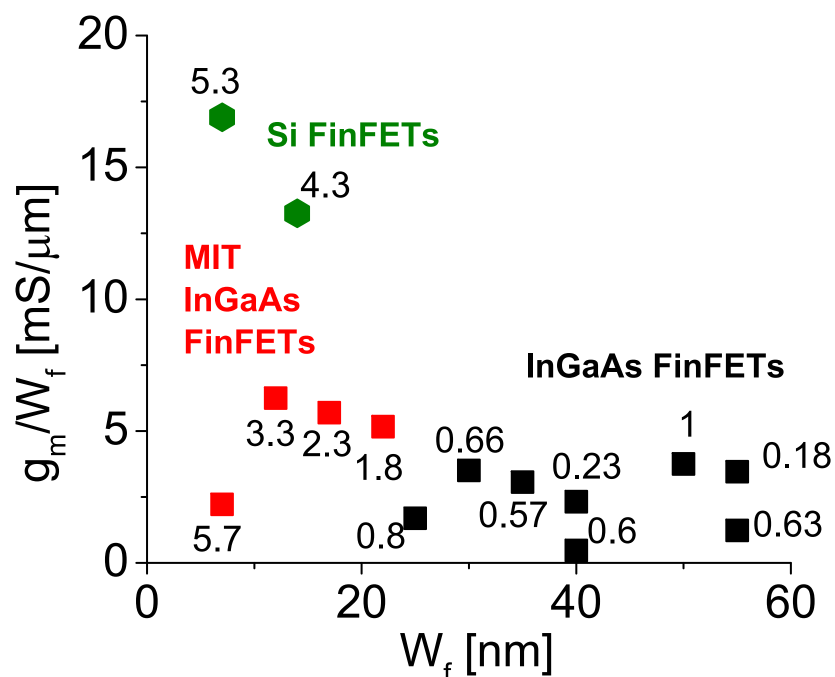
g_m per width of gate periphery



- First InGaAs FinFETs with W_f<10 nm
- First InGaAs FinFETs with channel aspect ratio >1

InGaAs FinFETs: g_m benchmarking

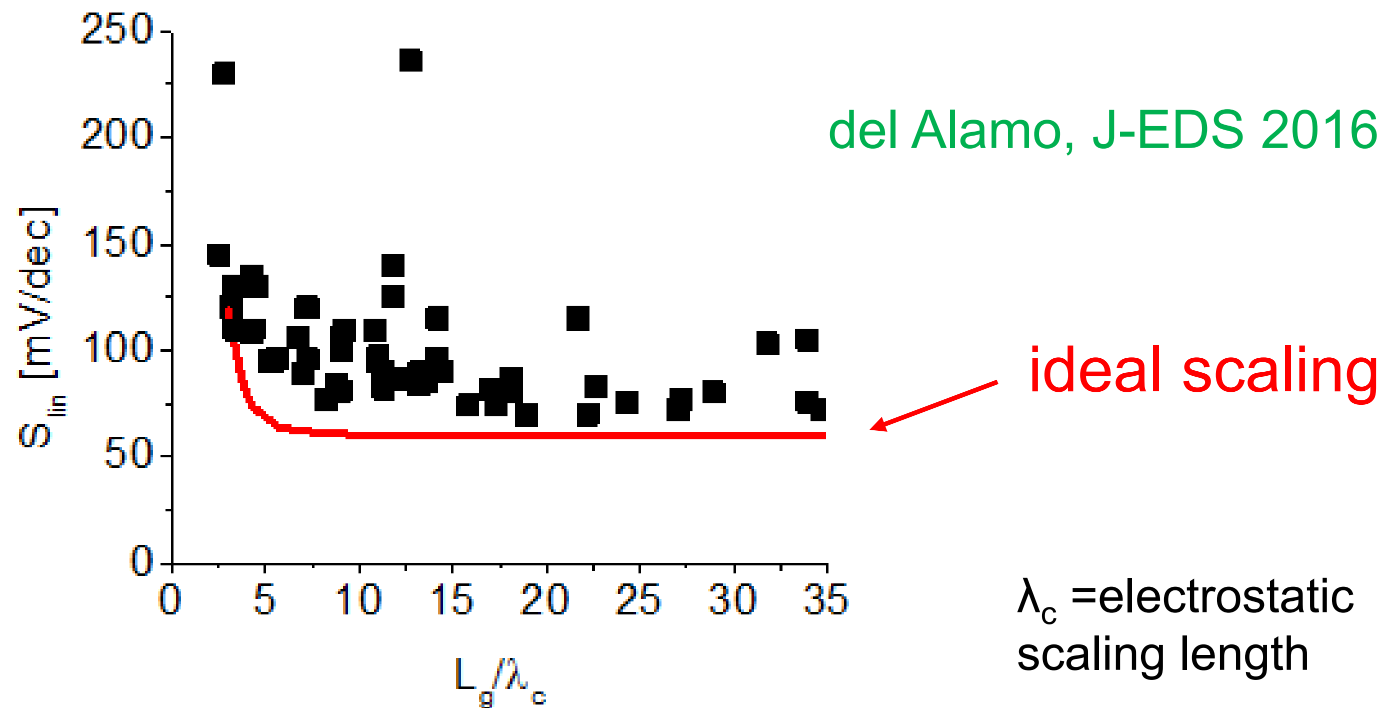
Figure-of-merit for density: g_m per fin width



- Improved by 50% over earlier InGaAs FinFETs
- Still far below Si FinFETs → poor sidewall charge control

InGaAs FinFETs: electrostatics

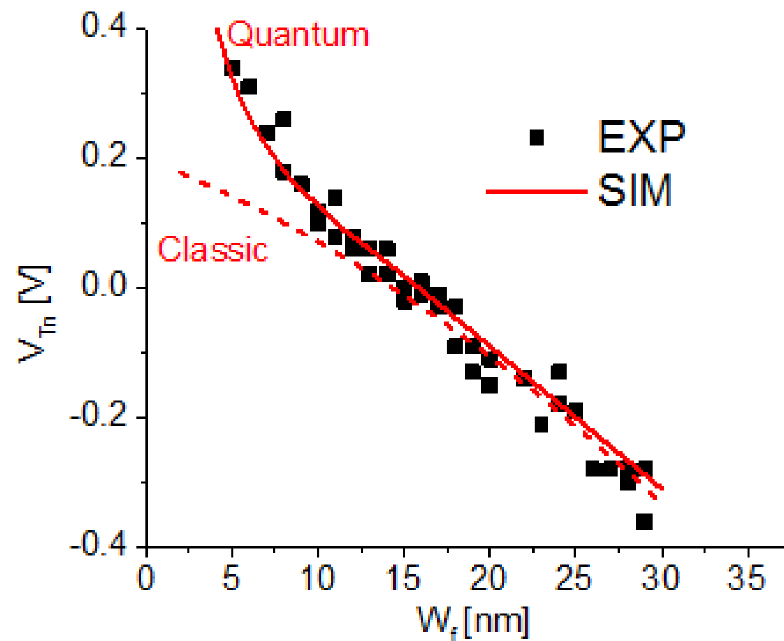
Linear subthreshold swing scaling:

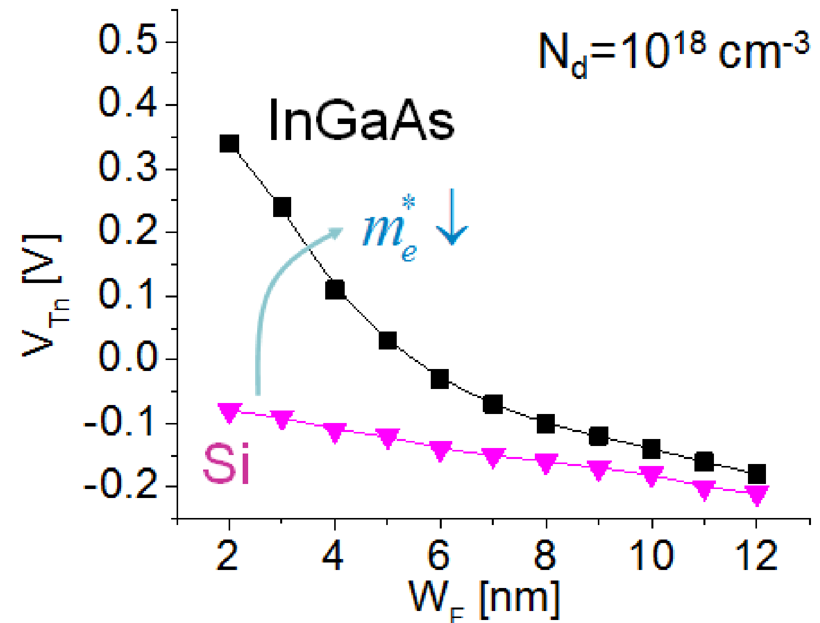


Close to ideal scaling reveals good quality sidewalls

Impact of fin width on V_T

InGaAs doped-channel FinFETs: 50 nm thick, N_D~10^{18} cm^{-3}
Oxide: Al_2O_3/HfO_2 (EOT~3 nm)

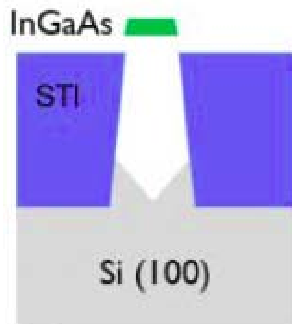


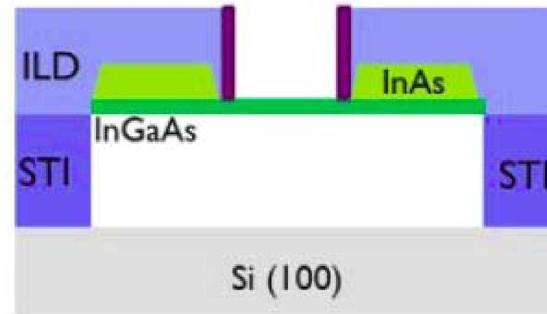


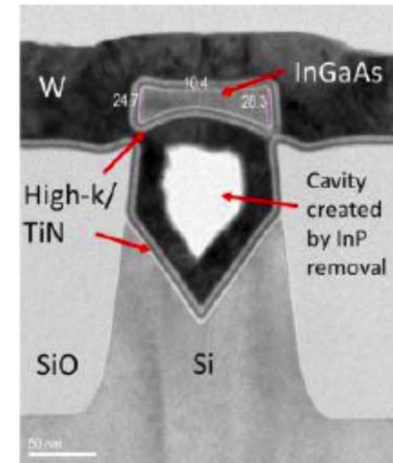
- Strong V_T sensitivity for W_f < 10 nm; much worse than Si
- Due to quantum effects

Vardi, IEDM 2015

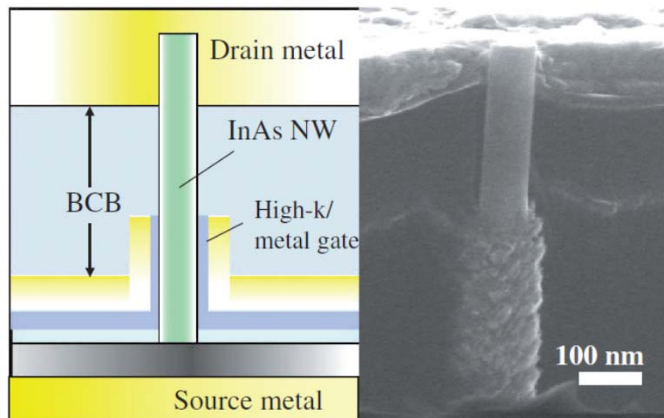
4. Nanowire InGaAs MOSFETs

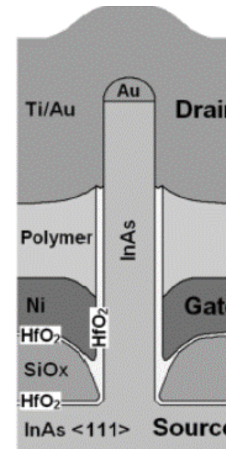


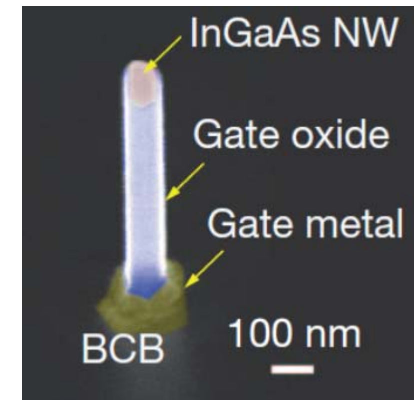




Waldron, EDL 2014



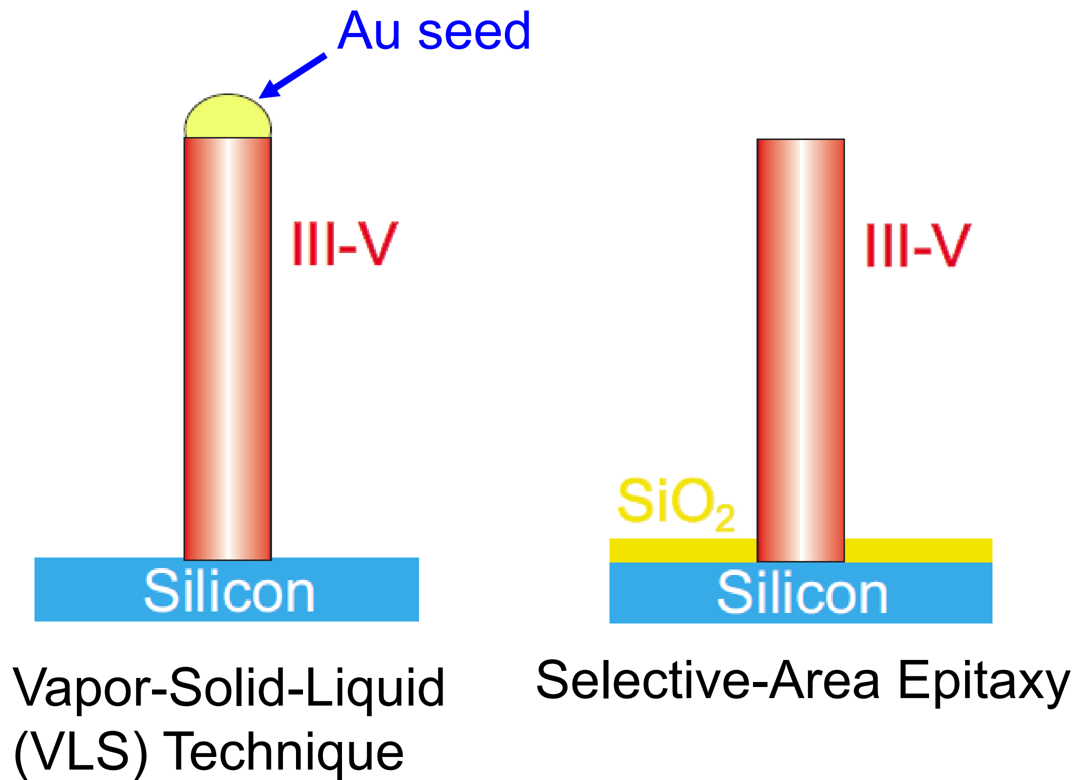




Tanaka, APEX 2010 Persson, EDL 2012 Tomioka, Nature 2012

- Nanowire MOSFET: ultimate scalable transistor
- Vertical NW: uncouples footprint scaling from L_g and L_c scaling

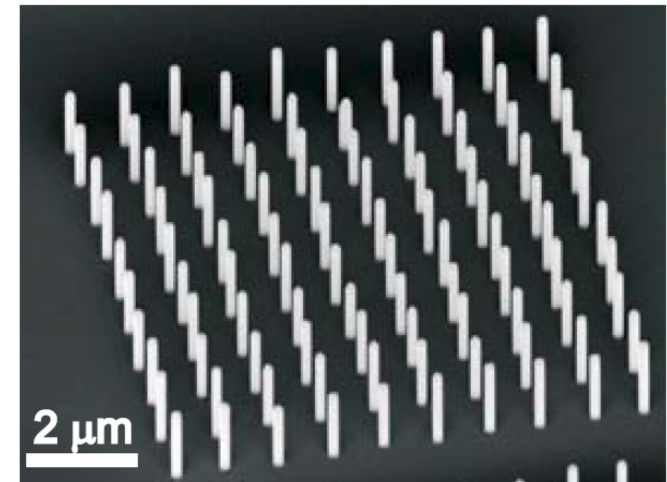
InGaAs Vertical Nanowires on Si by direct growth



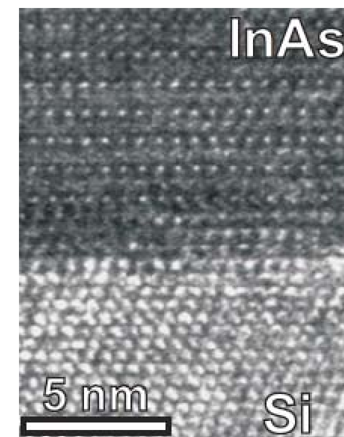
Vapor-Solid-Liquid (VLS) Technique

Selective-Area Epitaxy

Riel, MRS Bull 2014

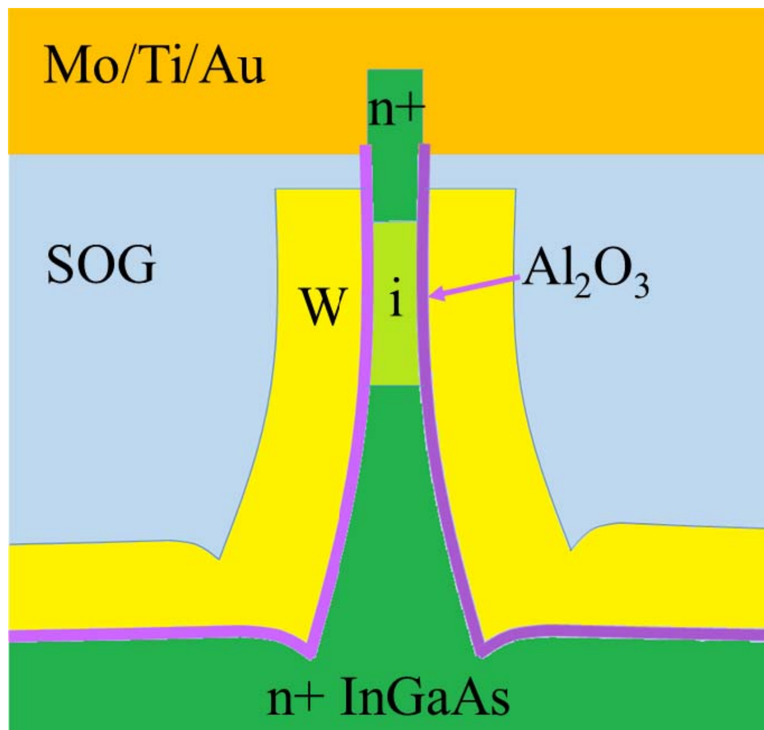


InAs NWs on Si by SAE

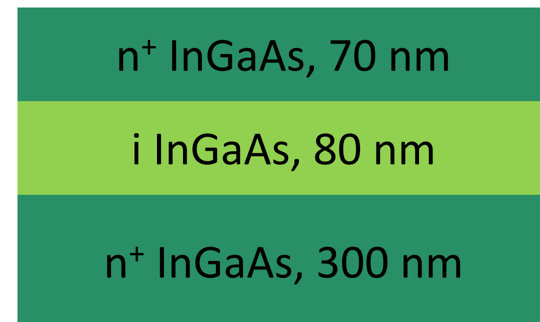


Björk, JCG 2012

InGaAs VNW-MOSFETs fabricated via top-down approach @ MIT



Starting heterostructure:



n^+: 6×10^{19} cm^{-3} Si doping

Top-down approach: flexible and manufacturable

Zhao, IEDM 2013

Key enabling technologies: RIE + digital etch

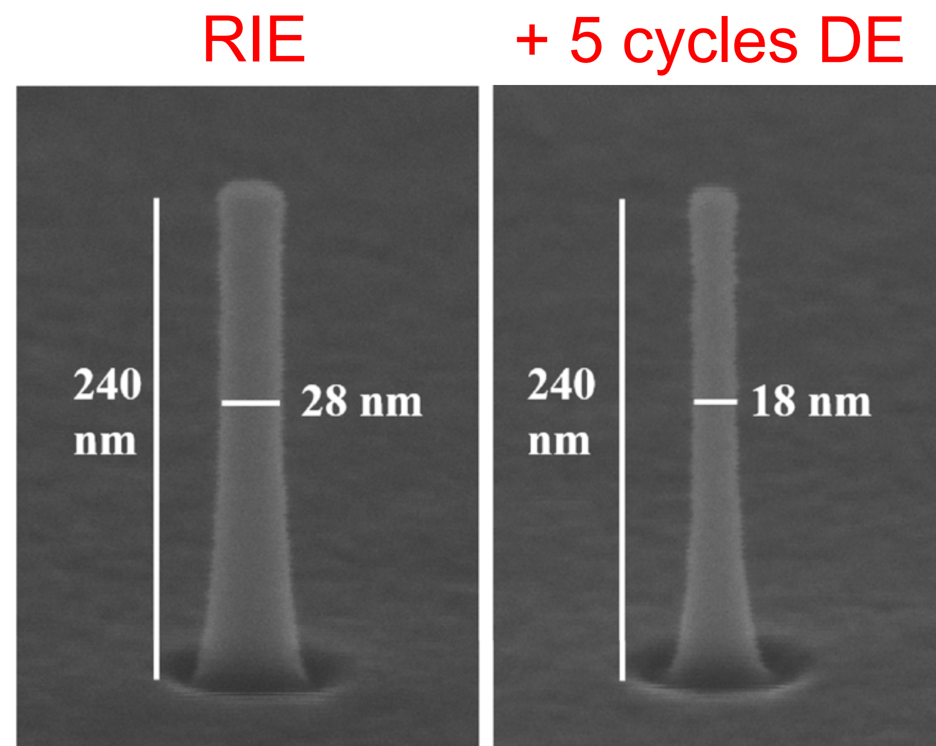
- RIE = $BCl_3/SiCl_4/Ar$ chemistry
- Digital Etch (DE) =

  self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal

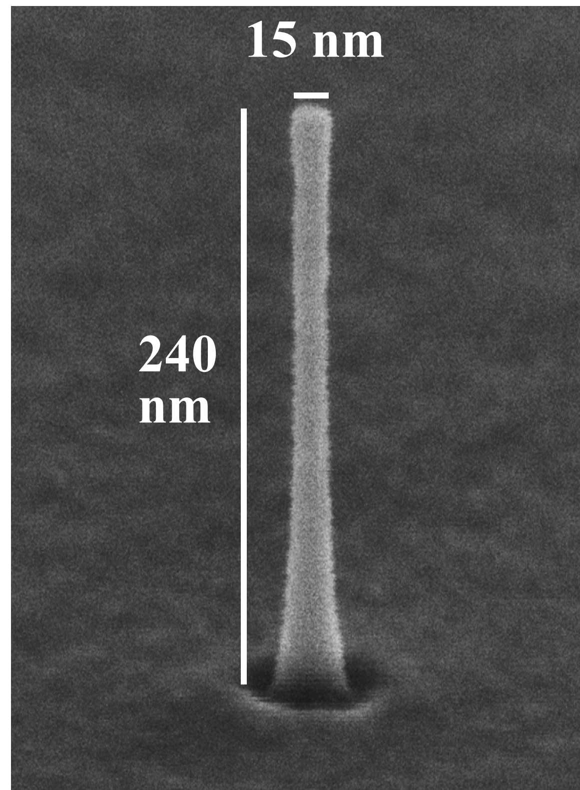
- Sub-20 nm NW diameter
- DE shrinks NW diameter by 2 nm per cycle
- Aspect ratio > 10
- Smooth sidewalls

Zhao, EDL 2014

RIE + 5 cycles DE



Optimized RIE + Digital Etch

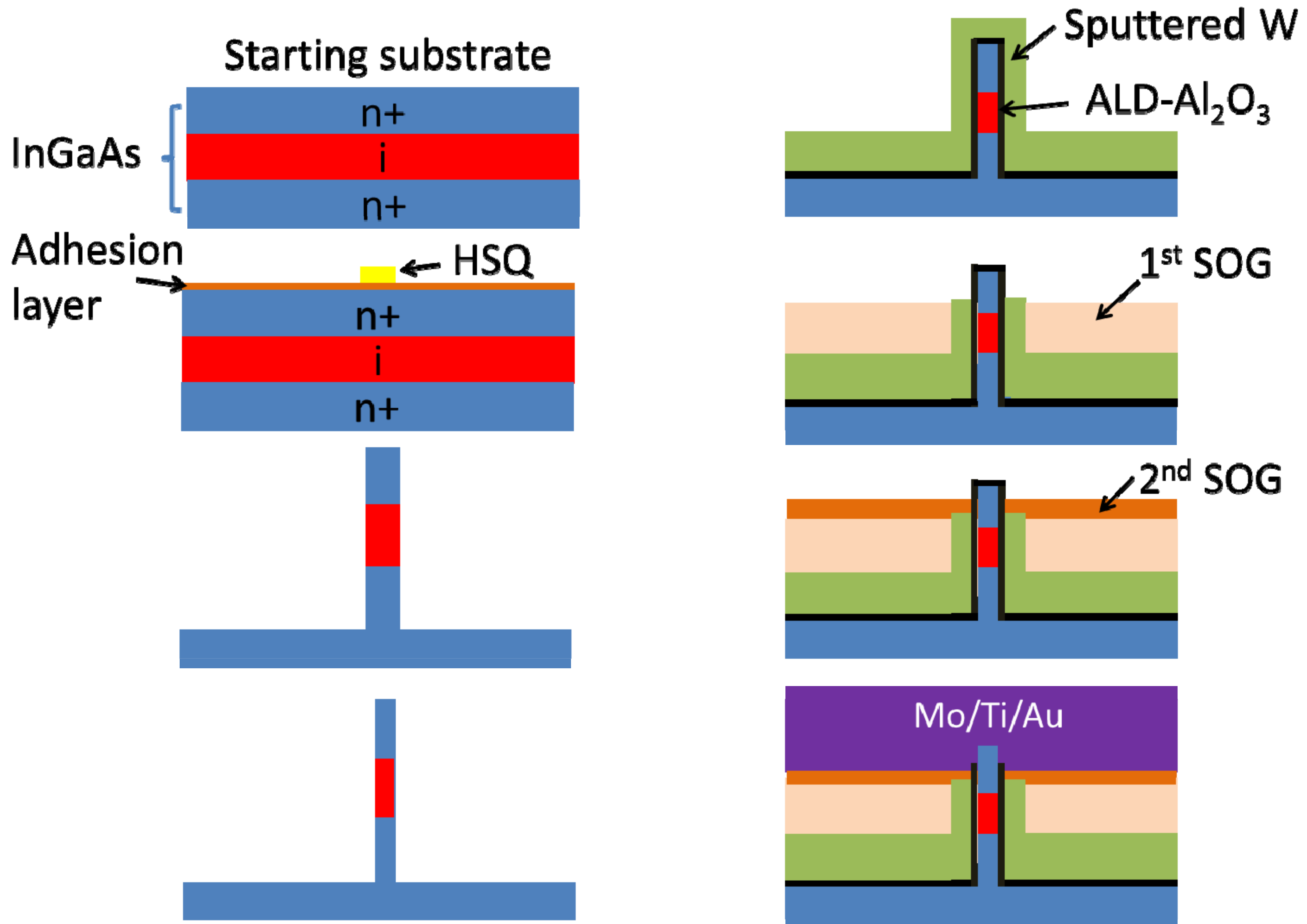


Zhao, EDL 2014

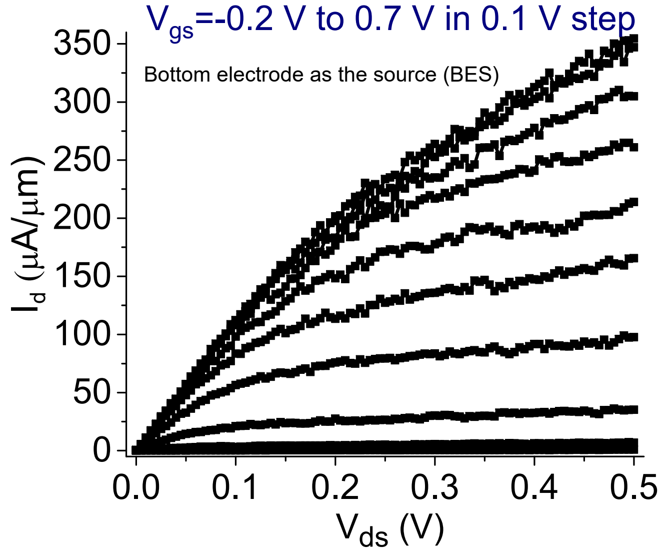
- Sub-20 nm resolution
- Aspect ratio = 16, vertical sidewall
- Smooth sidewall and surface

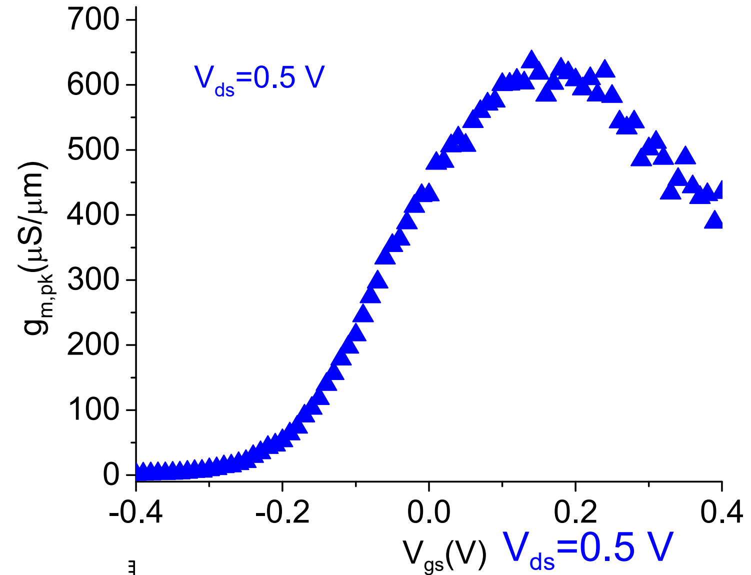
Tomioka, Nature 2012
Persson, DRC 2012

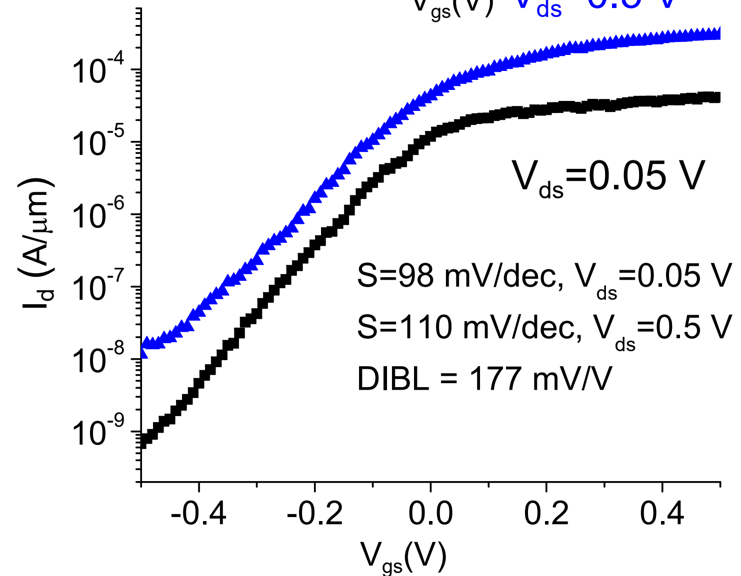
Process flow



NW-MOSFET I-V characteristics: D=40 nm





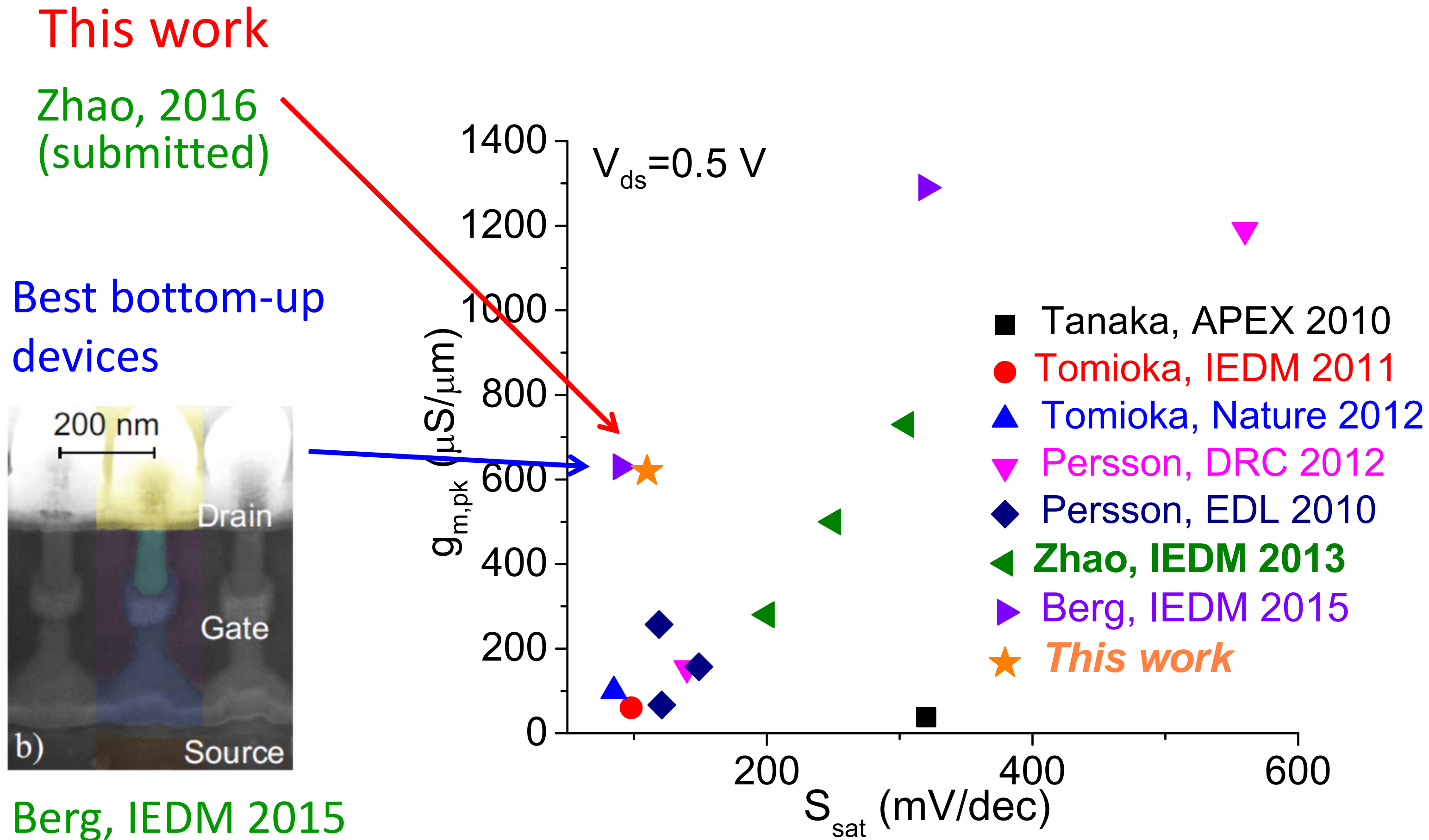


Single nanowire MOSFET:

- L_{ch}= 80 nm
- 3 nm Al_2O_3 (EOT = 1.5 nm)
- $g_{m,pk}$=620 μS/μm @ V_{DS}=0.5 V
- R_{on}=895 Ω.μm

Zhao, EDL 2016 (submitted)

Vertical InGaAs NW-MOSFETs Benchmark

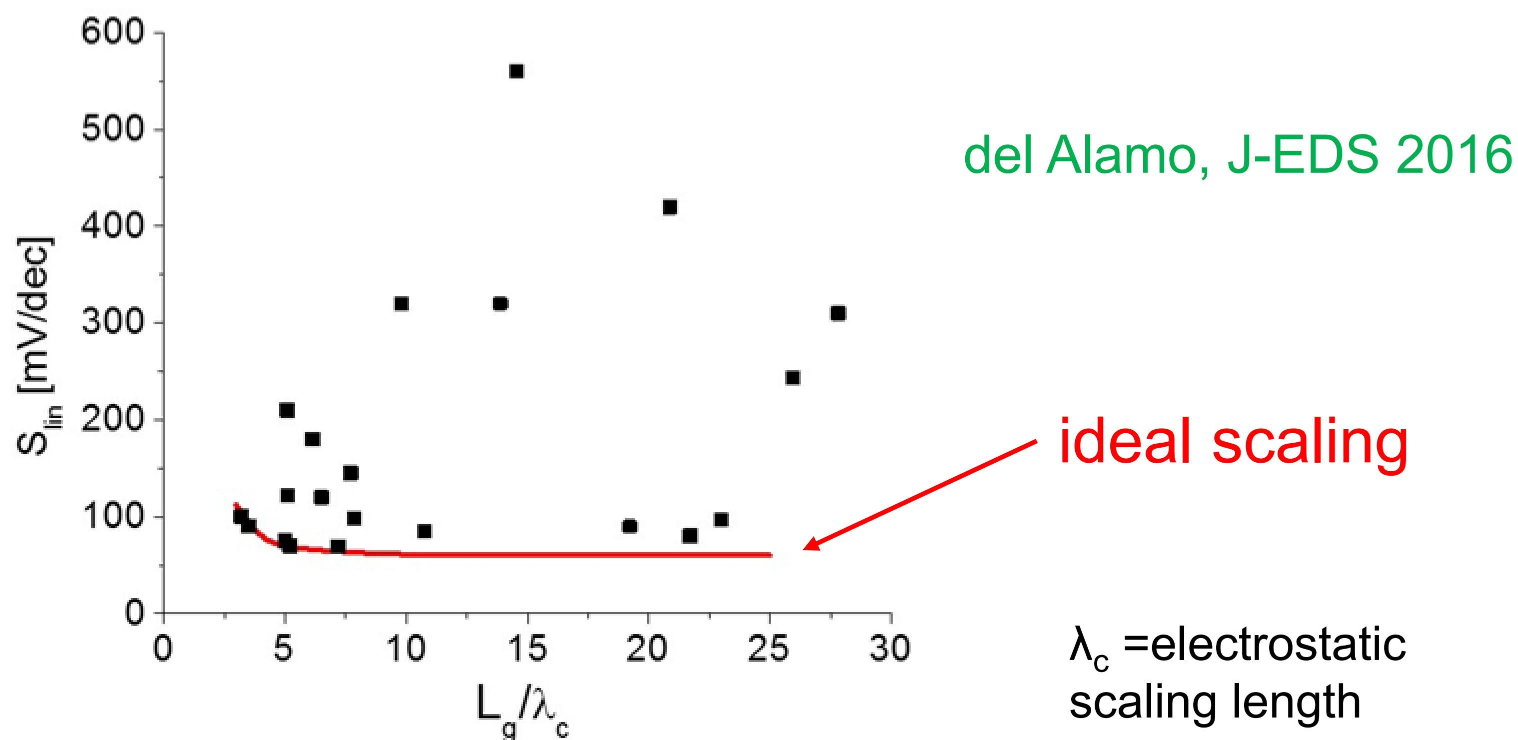


Berg, IEDM 2015

Top-down approach as good as bottom-up approach

InGaAs VNW MOSFETs: electrostatics

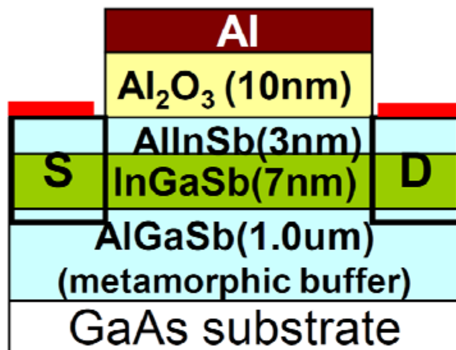
Linear subthreshold swing scaling:

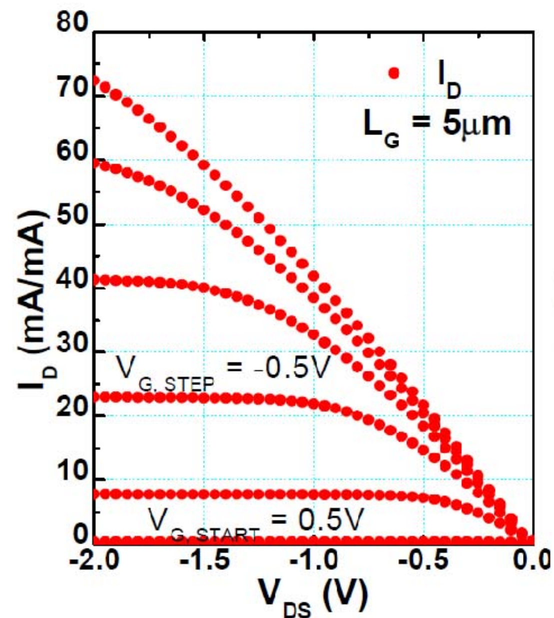


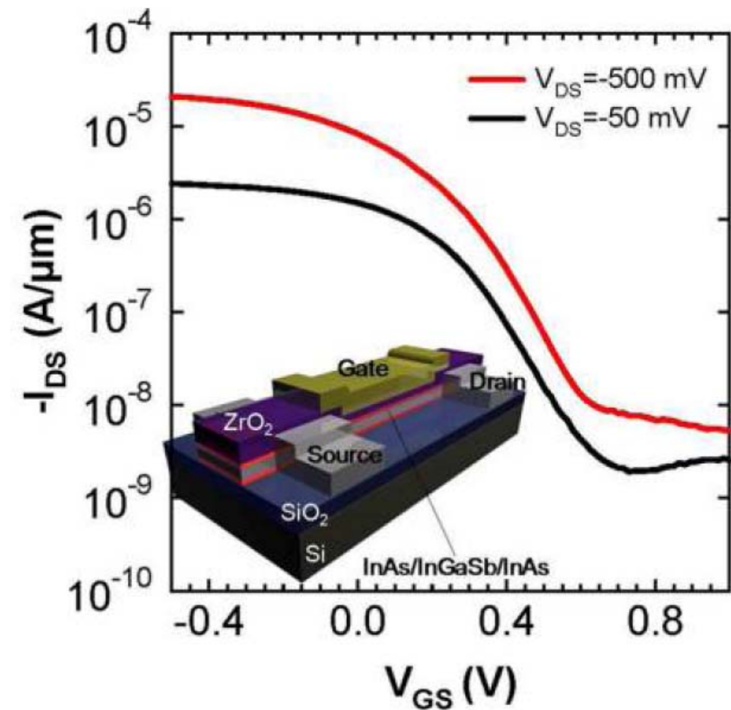
Close to ideal scaling reveals good quality sidewalls

5. InGaSb p–type MOSFETs

Planar InGaSb MOSFET demonstrations:







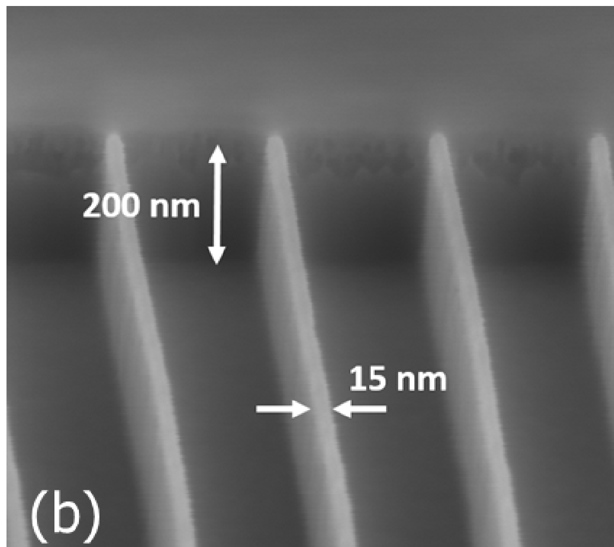
Nainani, IEDM 2010

Takei, Nano Lett. 2012

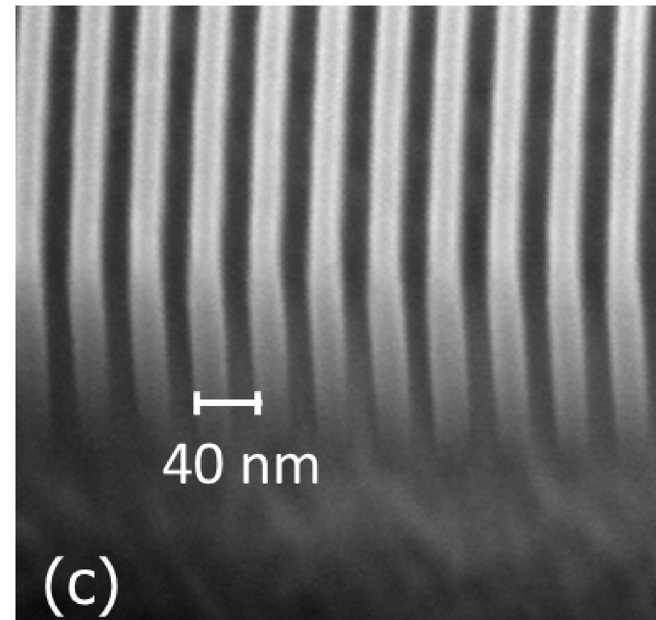
InGaSb p–type FinFETs at MIT

Key enabling technology:

- BCl_3/N_2 RIE
- [digital etch under development]



15 nm fins, AR>13



20 nm fins, 20 nm spacing

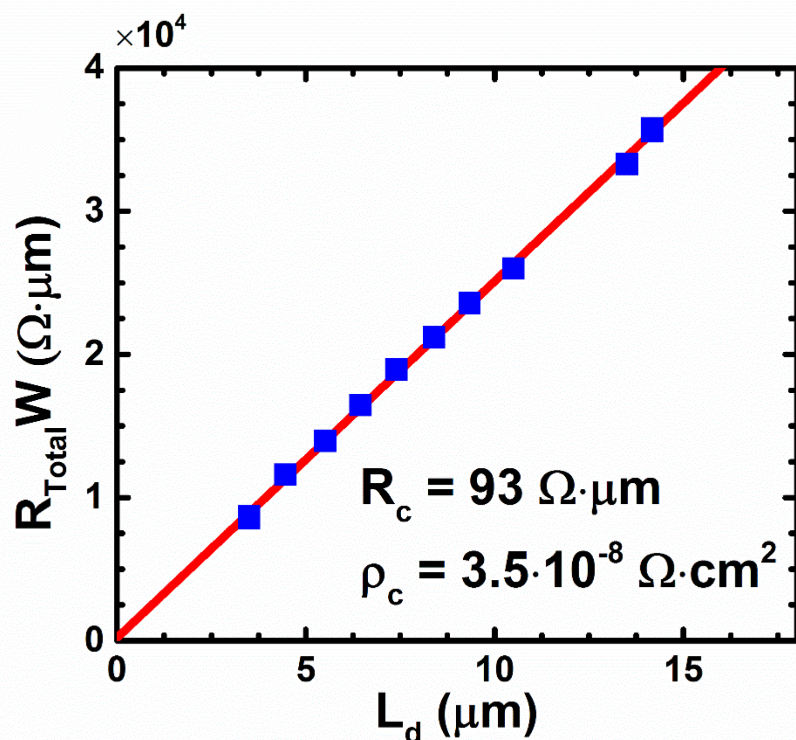
- Smallest W_f = 15 nm
- Aspect ratio >10
- Fin angle > 85°
- Dense fin patterns

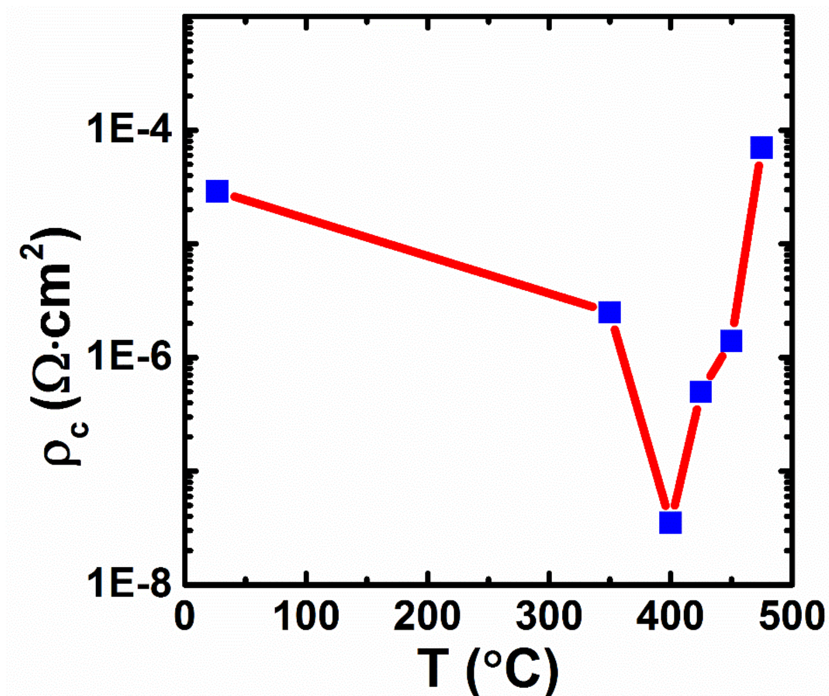
Lu, IEDM 2015

Si-compatible contacts to p^+-InAs

Ni/Ti/Pt/Al on p^+-InAs (circular TLMs):

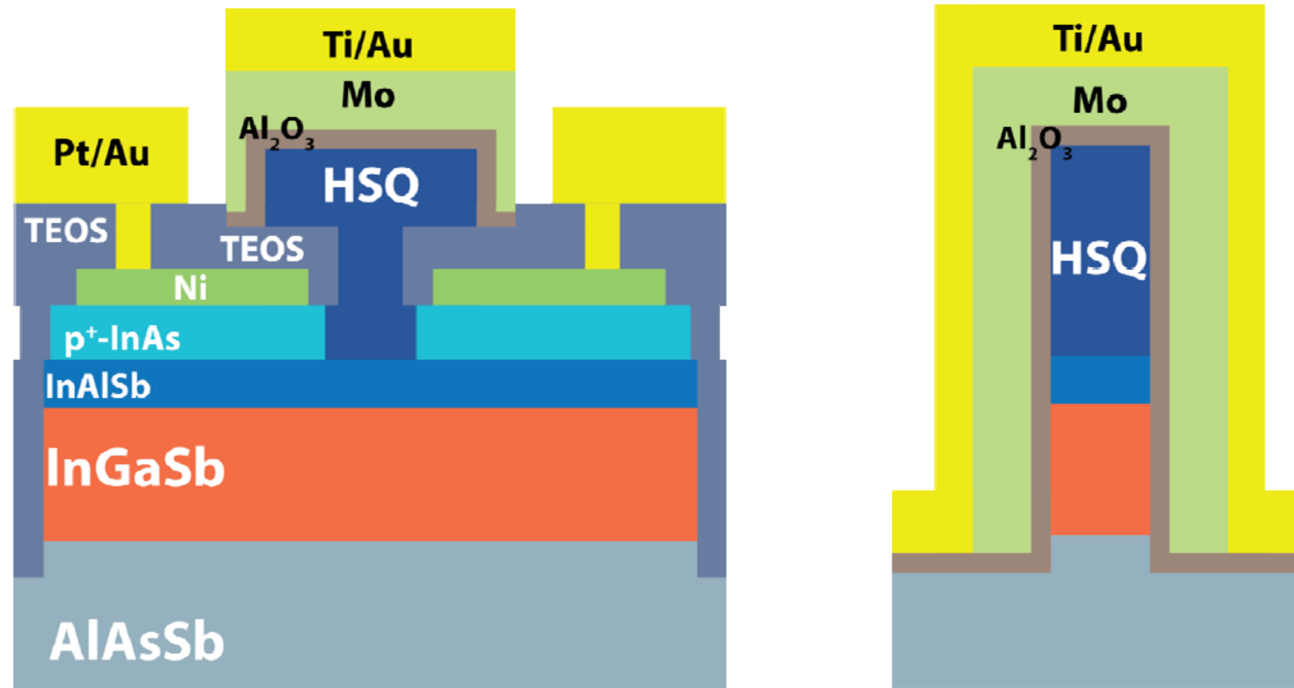
Lu, IEDM 2015





Record ρ_c: 3.5×10^{-8} Ω.cm^2 at 400°C

InGaSb FinFETs



Fin mask left in place → double-gate MOSFET

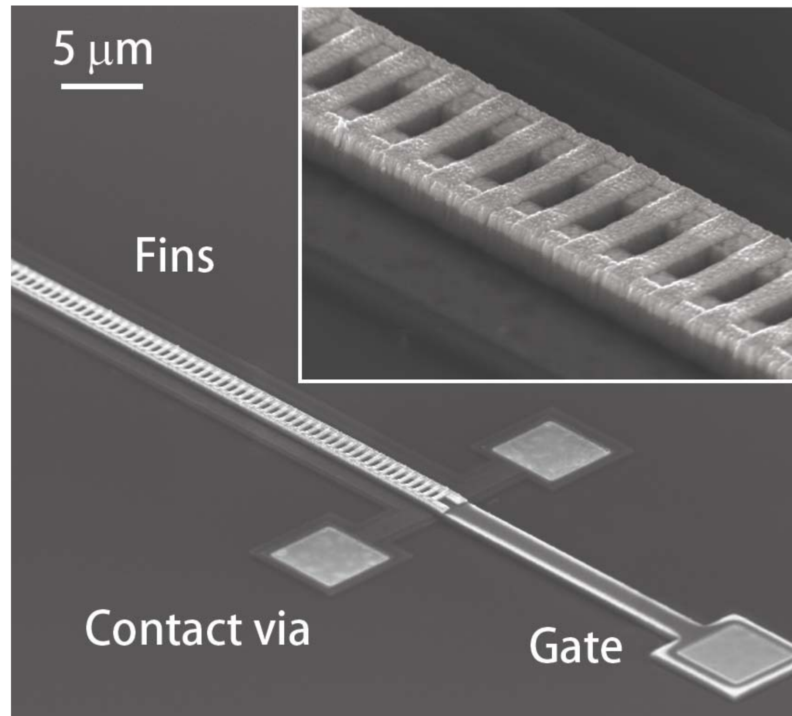
Channel: 10 nm $In_{0.27}Ga_{0.73}Sb$

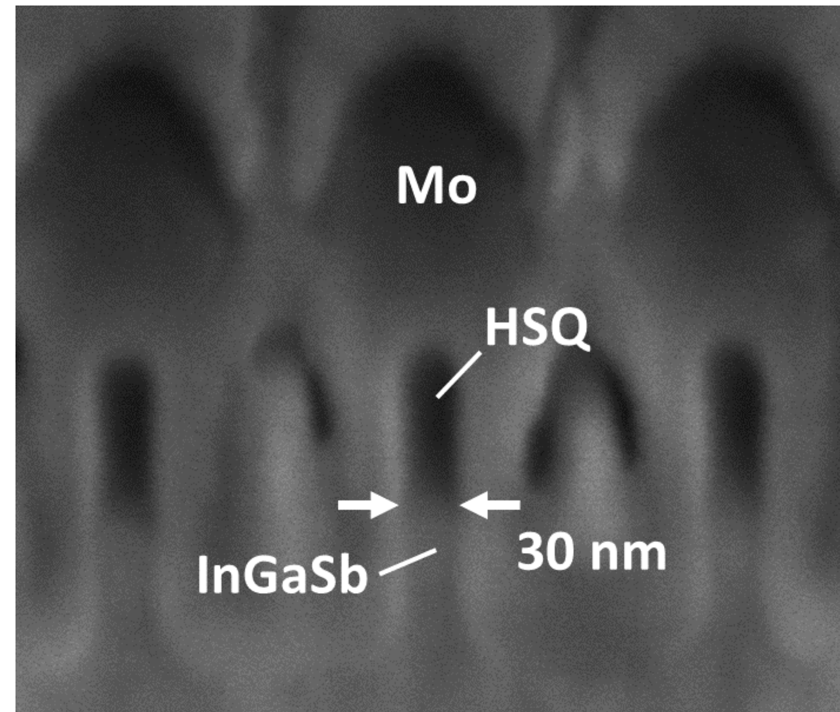
Gate oxide: 4 nm Al_2O_3 (EOT=1.8 nm)

Gate: 45 nm Mo

Lu, IEDM 2015

InGaSb FinFETs





W_f = 30 – 100 nm

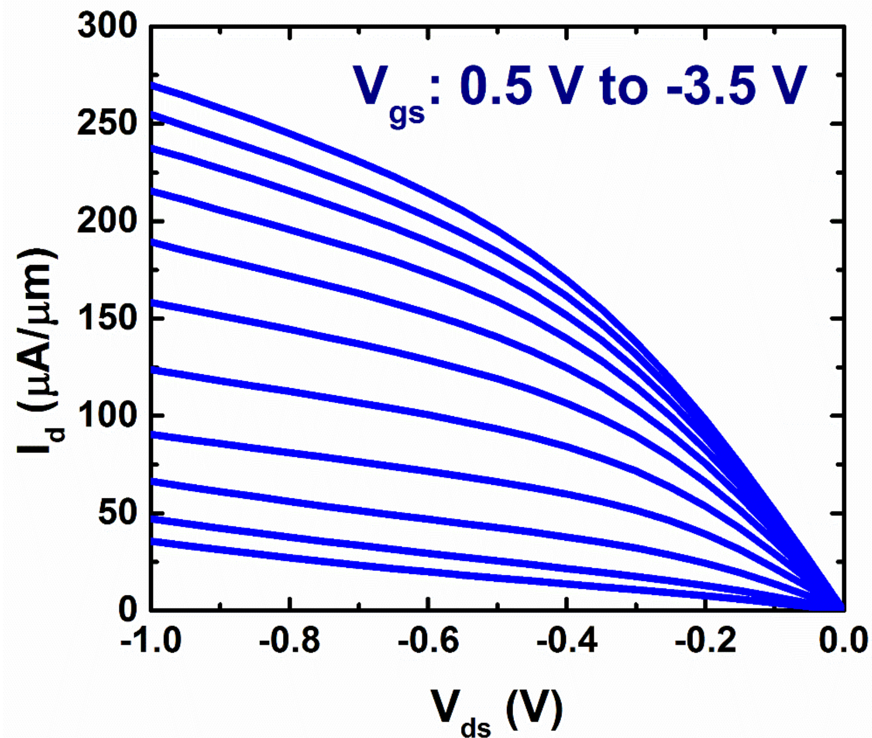
L_g = 0.1 – 1 μm

N_f = 70

Lu, IEDM 2015

InGaSb FinFET I-V characteristics

- L_g = 100 nm, W_f = 30 nm (AR=0.33)
- Normalized by conducting gate periphery

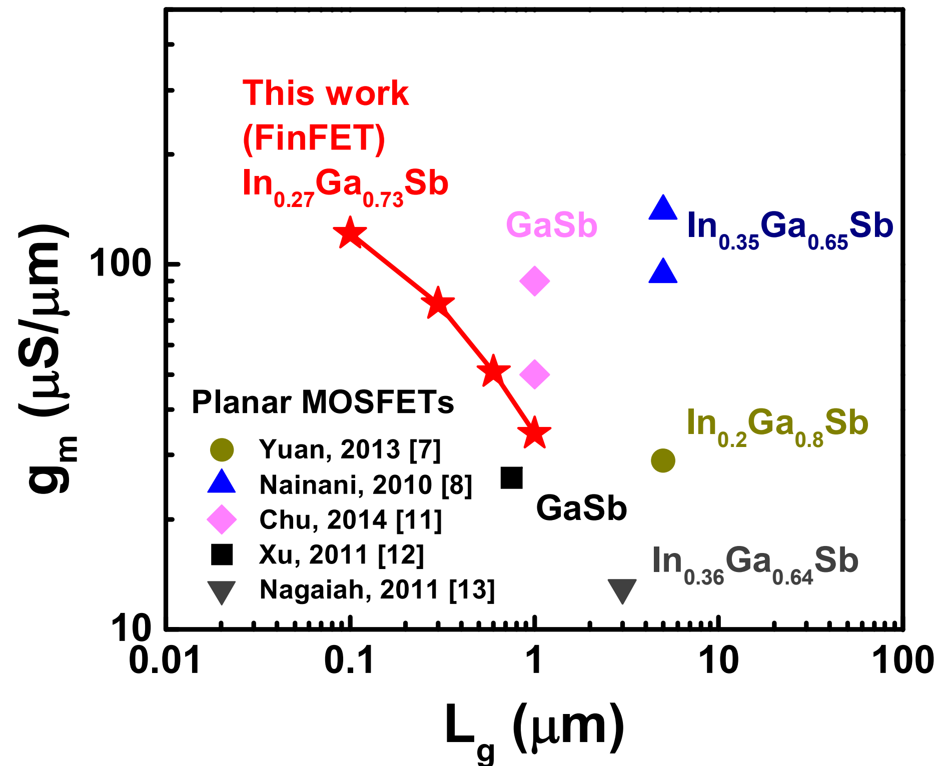


- High current
- Poor turn-off

Lu, IEDM 2015

g_m benchmarking

Peak g_m at T=290K:



Lu, IEDM 2015

- First InGaSb FinFET
- Peak g_m approaches best InGaSb planar MOSFETs

Conclusions

1. Great recent progress on planar, fin and nanowire III-V MOSFETs
2. Planar and multigate InGaAs MOSFETs exhibit nearly ideal electrostatic scaling behavior
3. Device performance still lacking for multigate designs
4. P-type InGaSb MOSFETs promising

A lot of work ahead but…
exciting future for III-V electronics